UCC28704 具有一次侧稳压 (PSR) 功能的高效离线 CV 和 CC 反激控制器

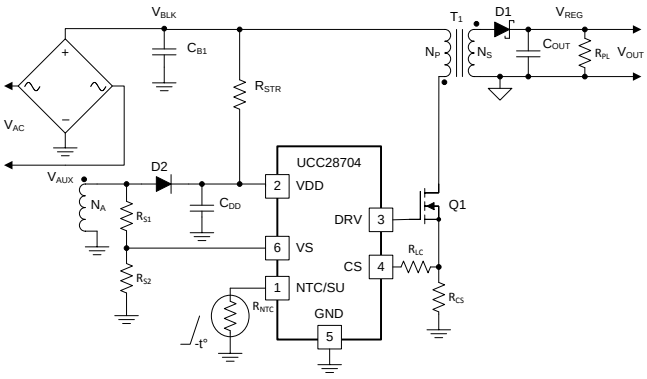
1 特性

- 效率超过 DoE VI 级和 EU CoC V5 Tier-2 外部电源标准
- 一次侧稳压功能免除了对光电耦合器和二次侧反馈组件的需求
- 与同步整流器兼容
- 无负载输入功率 <30mW
- ±5% 输出电压 (CV) 和电流 (CC) 调节
- 增强型动态负载响应
- 具有自动重启响应的恒流输出欠压保护 (CCUV)
- 电缆补偿（5V 满载时为 300mV）
- 85kHz 最大开关频率
- 断续导通模式 (DCM) 谷值开关运行
- 针对金属氧化物半导体场效应晶体管 (MOSFET) 的已钳位栅极驱动输出
- 负温度系数 (NTC) 电阻接口
- 电阻或外部高压 (HV) 耗尽型场效应晶体管 (FET) 启动
- 故障保护：输入欠压、输出过压、过流和短路保护
- 小外形尺寸晶体管 (SOT) 23-6 封装

2 应用

- 手机和平板电脑的适配器和充电器
- 消费类电子产品的 USB Type-C 交流适配器
- 低功率 AC 至 DC 开关模式电源 (SMPS)
- 工业用和医疗用开关模式电源 (SMPS)

LP38690 的



3 说明

UCC28704 离线反激控制器是一款高度集成的 6 引脚一次侧稳压脉宽调制 (PWM) 控制器，旨在设计符合全球效率标准的高效 AC 转 DC 电源。此控制器启动时的电流消耗超低，可使设计获得低于 30mW 的无负载输入功率，并且节省待机模式能耗。凭借智能一次侧感应和控制功能，无需使用光电耦合器或二次侧反馈电路即可将输出电压和电流控制在 5% 的变化范围内。

UCC28704 应用了增强型负载瞬态响应技术，有助于最大限度减小输出电容，从而减小系统整体尺寸并降低成本。此外，该控制器还免除了对环路补偿组件的需求，为电源设计人员简化了设计及调试过程。转换器的输出电压和电流会得到稳定性处理，以防出现可能损坏负载或连接器的过载状况。同样，恒流输出欠压保护 (CCUV) 关断特性会监控输出欠压故障以防止由于软短路问题而造成连接器过热或烧毁，从而大幅度提升系统整体可靠性。NTC 接口引脚有助于为电路板或组件施加过热保护。

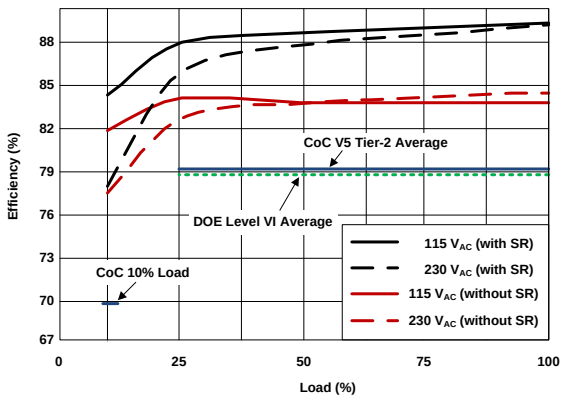
UCC28704 在 2A 或更高输出电流下可轻松与 TI 的二次侧同步整流器 (SR) 控制器搭配使用，从而提高转换效率或实现更为紧凑的设计。

器件信息 (1)

部件号	封装	封装尺寸（标称值）
UCC28704	SOT23-6	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

5V/2A 适配器效率



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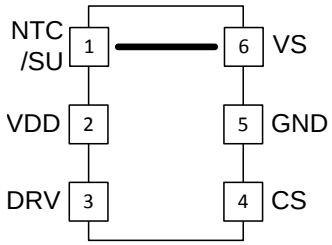
4 修订历史记录

日期	修订版本	注释
2016 年2 月	A	首次发布。

5 Pin Configuration and Functions

SOT23-6 Package
6-Pin DBV
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
NTC/SU	1	I/O	NTC/SU is a multi-function pin. First, it provides an interface to an external NTC (negative temperature coefficient) resistor for remote temperature sensing. Pulling this pin low shuts down PWM action. Additionally, when used with an external depletion-mode FET and a low-voltage NPN transistor this pin provides high-voltage start up control. A maximum 100-pF noise filter capacitance may be added to this pin. The pin should be left floating if not used.
VDD	2	P	VDD is the bias supply input pin to the device.
DRV	3	O	DRV is an output pin used to drive the gate of an external high voltage MOSFET switching transistor.
CS	4	I	CS input connects to a ground referenced current sense resistor in series with the power switch. The resulting voltage is used to monitor and control the peak-primary current. A series resistor is added to this pin to compensate the peak-primary current levels as the AC mains input varies. A small capacitance, up to 30 pF, can be added to this pin to filter the current sense signal.
GND	5	G	GND pin is both the reference pin for the controller and the low-side return for the drive output. Special care should be taken to return all AC decoupling capacitors as close as possible to this pin and avoid any common-mode signal trace length with analog signal return paths.
VS	6	I	VS is an input used to provide voltage and timing feedback to the controller. This pin is connected to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider is used to program the AC-mains run-and-stop thresholds and line compensation at the CS pin. Avoid placing a filter capacitor on this input which would interfere with accurate sensing of this waveform.

(1)

P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{VDD}	Bias supply voltage		38	V
VS	Voltage range	–0.75	7	V
CS, NTC	Voltage range	–0.5	5	V
V_{DRV}	Gate-drive voltage at DRV	–0.5	Self-limiting	V
I_{DRV}	DRV continuous sink current		50	mA
I_{DRV}	DRV peak sourcing current, V_{DRV} = 10 V to 0 V		Self-limiting	mA
I_{DRV}	DRV peak sink current, V_{DRV} = 0 V to 10 V		Self-limiting	mA
I_{VS}	VS, peak, 1% duty-cycle, when detecting line voltage		1.2	mA
T_J	Operating junction temperature range	–55	150	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature 0.6 mm from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM) ESD stress voltage (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VDD	Bias supply operating voltage	8.5	35	V
C_{DD}	VDD bypass capacitor	0.047	no limit	µF
I_{VS}	VS pin sourcing current when detecting line voltage		1.0	mA
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC		UCC28704 DBV 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance (1)	150	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (2)	55	°C/W
θ_{JB}	Junction-to-board thermal resistance (3)	60	°C/W
ψ_{JT}	Junction-to-top characterization parameter (4)	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter (5)	55	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

6.5 Electrical Characteristics

Over operating free-air temperature range, V_{VDD} = 25 V, R_{NTC} = open, –40°C ≤ T_A ≤ 125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state	1.65	2.3	2.65	mA
I_{WAIT}	Supply current, wait	I_{DRV} = 0, V_{VDD} = 20 V, wait state	40	70	100	µA
I_{START}	Supply current, start	I_{DRV} = 0, V_{VDD} = 17 V, start state		1.5	2.5	µA
I_{FAULT}	Supply current, fault	I_{DRV} = 0, fault state	1.7	2.2	2.8	mA
UNDER-VOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turn-on threshold	V_{VDD} low to high	17.5	21	23	V
$V_{VDD(off)}$	VDD turn-off threshold	V_{VDD} high to low	7.3	7.7	8.15	V
VS INPUT						
V_{VSR}	Regulating level (1)	Measured at no-load condition, T_J = 25°C	4.02	4.06	4.1	V
V_{VSNC}	Negative clamp level	I_{VS} = –300 µA	190	250	325	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	–0.25	0	0.25	µA
CS INPUT						
$V_{CST(max)}$	Max CS threshold voltage (2)	V_{VS} = 3.70 V	720	750	784	mV
$V_{CST(min)}$	Min CS threshold voltage (2)	V_{VS} = 4.35 V	170	187.5	210	mV
K_{AM}	AM control ratio	$V_{CST(max)}$ / $V_{CST(min)}$	3.55	4	4.4	V/V
V_{CCR}	Constant-current regulating level		345	356	369	mV
K_{LC}	Line compensating current ratio, I_{VSLS} / (current out of CS pin)	I_{VSLS} = –300 µA	23	25	29	A/A
T_{CSLEB}	Leading-edge blanking time	DRV output duration, V_{CS} = 1 V	170	255	340	ns

(1) The regulation level and OV threshold at VS decrease with increasing temperature by 1 mV/°C. This compensation over temperature is included to reduce the variances in power supply output regulation over-voltage detection with respect to the external output rectifier.
(2) These threshold voltages represent average levels. This device automatically varies the current sense threshold to improve EMI performance.

Electrical Characteristics (continued)

Over operating free-air temperature range, V_{VDD} = 25 V, R_{NTC} = open, –40°C ≤ T_A ≤ 125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRV						
I_{DRS}	DRV source current	V_{DRV} = 5 V, V_{VDD} = 9 V	25	32	38	mA
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 10 mA		6.5	12	Ω
V_{DRCL}	DRV clamp voltage	V_{VDD} = 35 V	9.5	10.6	13	V
R_{DRVSS}	DRV pull-down in start state		165	205	250	kΩ
TIMING						
$f_{SW(max)}$	Maximum switching frequency (3)	V_{VS} = 3.7 V	78	85	94	kHz
$f_{SW(min)}$	Minimum switching frequency	V_{VS} = 4.6 V	0.88	1.03	1.18	kHz
t_{ZTO}	Zero-crossing timeout delay		1.7	2.39	3	µs
t_{CCUV_BLANK}	Blanking delay time before CCUV shutdown	V_{VS} step from 3.5 V to 2.4 V to DRV stop switching	90	120	150	ms
PROTECTION						
K_{OVP}	Over-voltage threshold ratio to V_{VSR}	V_{OVP}/V_{VSR}	1.13	1.15	1.18	V/V
V_{CCUV}	CCUV V_O = 3.0 V	T_J = 25℃, auto restart after fault	2.41	2.48	2.55	V
V_{OCP}	Over-current threshold	At CS input	1.35	1.51	1.6	V
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin – increasing	190	220	265	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin – decreasing	70	80	100	µA
K_{VSL}	VS line-sense ratio $I_{VSL(run)}$ / $I_{VSL(stop)}$		2.55	2.8	2.95	A/A
$T_{J(stop)}$	Thermal shut-down temperature (4)	Internal junction temperature		150		°C
CABLE COMPENSATION						
$V_{CVS(max)}$	Maximum compensation at VS	Change in VS regulating level at full-load	180	220	260	mV
NTC INPUT						
V_{NTCTH}	NTC shut-down threshold	VDD UVLO cycle when below this threshold	0.9	0.95	1	V
I_{NTC}	NTC pull-up current, out of pin	V_{NTC} = 1.1 V	90	100	120	µA

(3) These frequency limits represent average levels. This device automatically varies the switching frequency to improve EMI performance.
(4) Not tested in production.

6.6 Typical Characteristics

VDD = 25 V, unless otherwise noted.

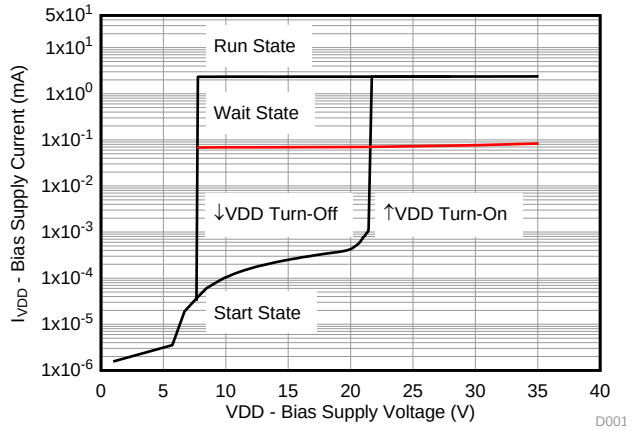


图 1. Bias Supply Current vs. Bias Supply Voltage

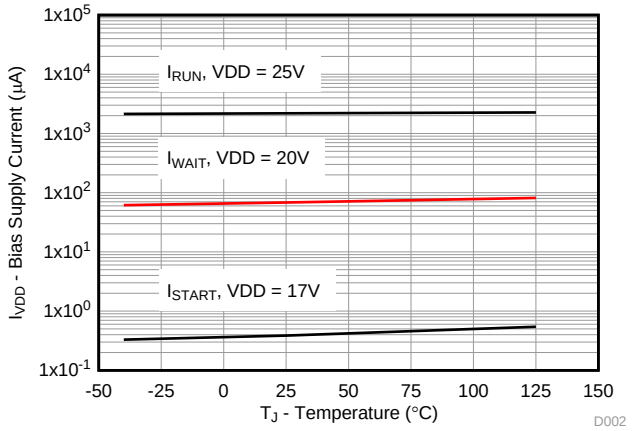


图 2. Bias Supply Current vs. Temperature

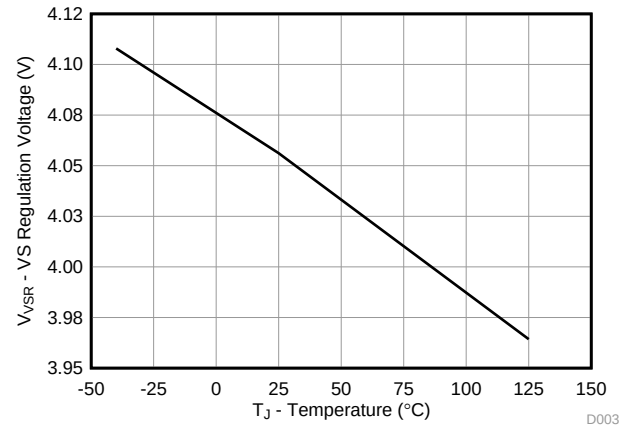


图 3. VS Regulation Voltage vs. Temperature

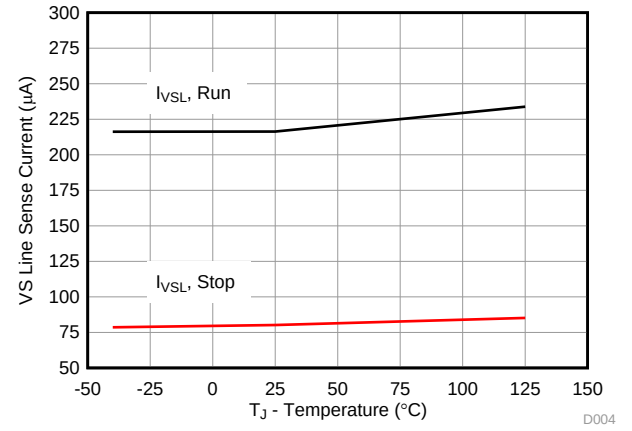


图 4. Line-Sense Current vs. Temperature

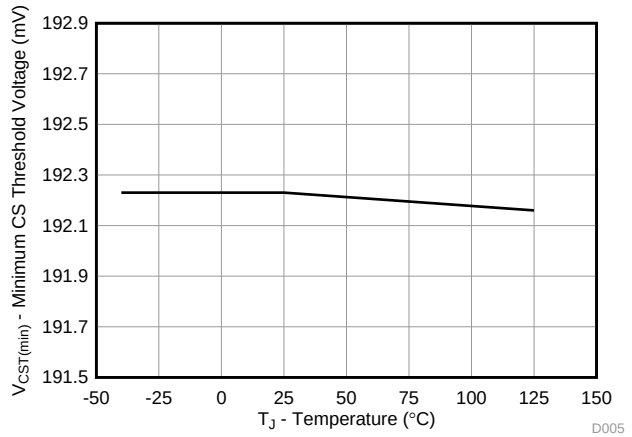


图 5. Minimum CS Threshold Voltage vs. Temperature

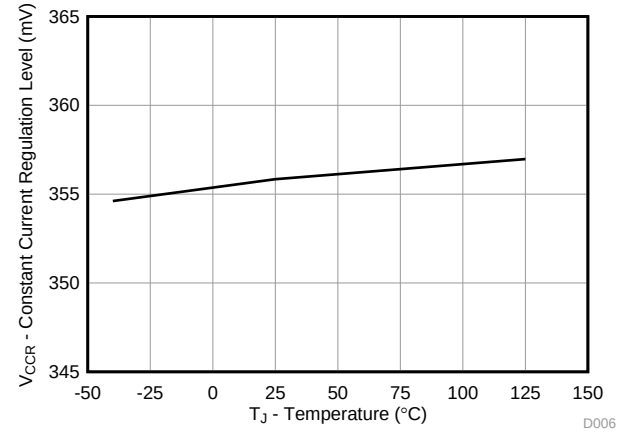


图 6. Constant-Current Regulation Level vs. Temperature

Typical Characteristics (接下页)

VDD = 25 V, unless otherwise noted.

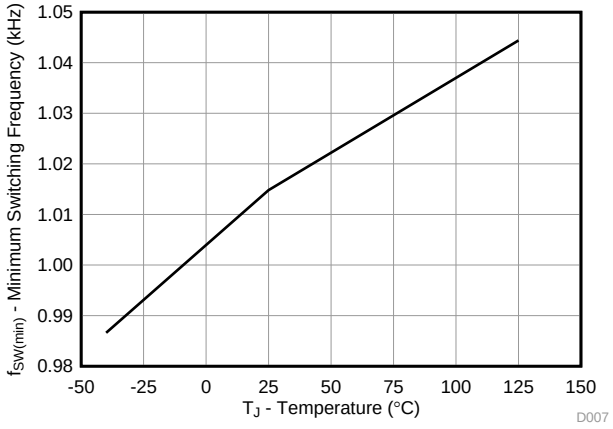


图 7. Minimum Switching Frequency vs. Temperature

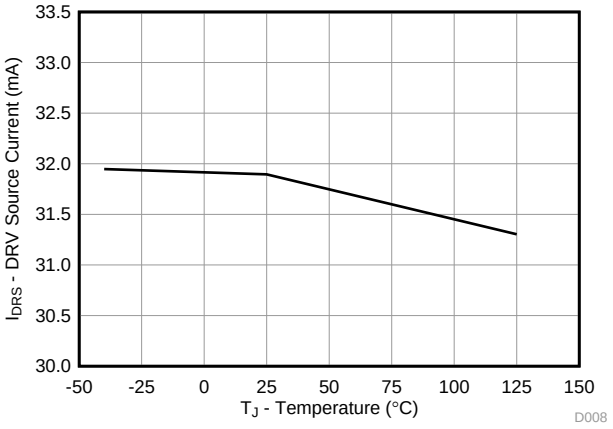


图 8. DRV Source Current vs. Temperature

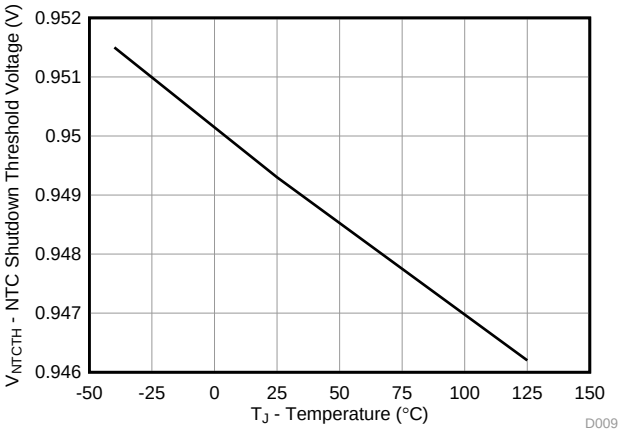


图 9. NTC Shutdown Threshold Voltage vs. Temperature

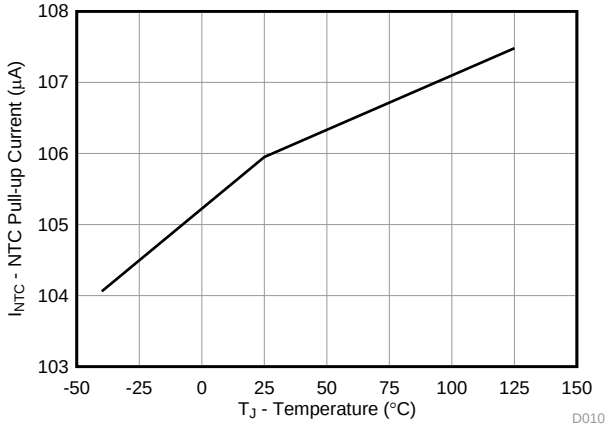


图 10. NTC Pullup Current vs. Temperature

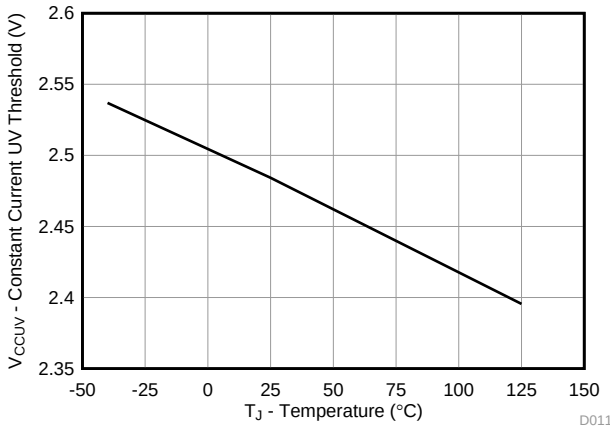


图 11. Constant-Current Under-Voltage Threshold vs. Temperature

7 Detailed Description

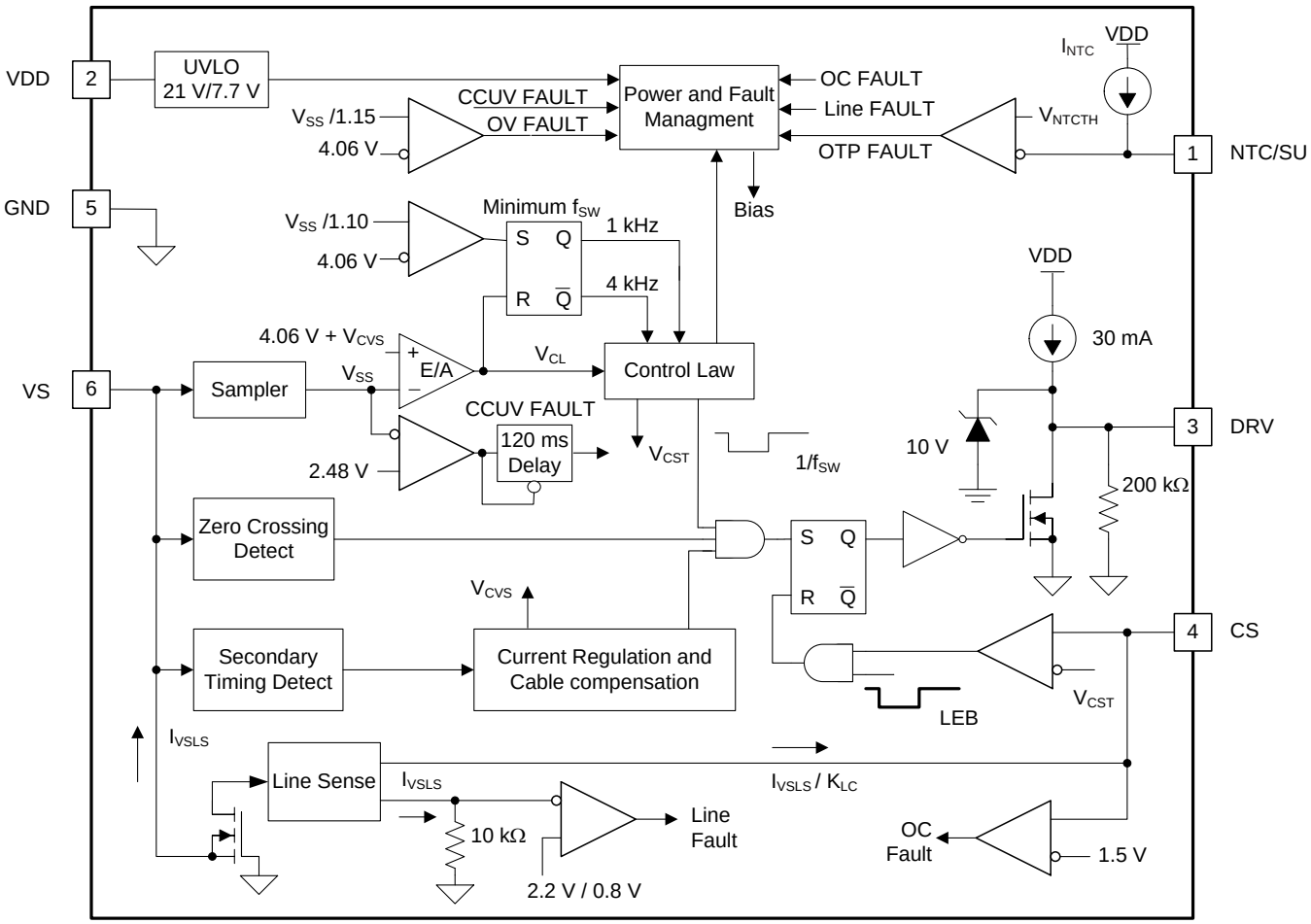
7.1 Overview

The UCC28704 flyback power supply controller provides accurate constant voltage and constant current regulation with primary-side feedback control. It also eliminates the need for opto-coupler feedback circuits. The controller optimizes the modulation scheme and the device's power management to boost power conversion efficiency, lower power dissipation at no-load and light load. Frequency dithering reduces the EMI peak energy at the fundamental switching frequency and harmonics. Features include fixed cable compensation and constant current output under-voltage shutdown, or CCUV, to protect USB terminals from getting over-heated or burn-out condition during soft-short circuit fault.

The controller operates in discontinuous conduction mode with valley switching to minimize switching losses. A combination of frequency modulation and primary peak current modulation to provide high power conversion efficiency across the load range. Accurate voltage and constant current regulation, fast dynamic response, and fault protection are achieved with primary-side control. A complete charger solution can be realized with a straightforward design process, low cost and low component count.

In UCC28704, as compared to UCC28700/1/2/3, features such as constant current under voltage protection and enhanced load transient schemes have been added. Also, in UCC28704, the demagnetizing ratio has been extended to 0.475 along with an increased AM ratio of 4:1. The maximum frequency of the controller is set at 85 kHz and the AM region switching frequency is optimally set at 25 kHz to have better trade-offs between no-load standby power consumption and load transient response. UCC28704 also incorporates schemes to have better noise rejection at the output voltage sense (VS pin) allowing for improved output voltage ripple reduction.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Detailed Pin Description

7.3.1.1 VDD (Device Bias Voltage Supply)

The VDD pin is typically powered from a rectified auxiliary transformer winding, the same winding that is used to capture the output voltage level. A bypass capacitor, with minimum value 0.047 µF, on the VDD pin is used for initially biasing the device to start-up along with a resistive or active source of start-up charging current. UVLO start / stop levels of 21 V / 7.7 V accommodate lower values of VDD capacitance that in turns keeps the start-up current low, which for resistive start-up has an impact on both stand-by power and power-on delay. A high, 35-V, maximum operating level on VDD alleviates concerns with leakage energy charging of VDD and gives added flexibility to when varying power supply output voltage must be supported.

7.3.1.2 GND (Ground)

This is an external return pin, and provides the reference point for both external signal and the gate drive of the device. The VDD bypass capacitor should be placed close to this pin. Critical component GND connections from the VS, CS and NTC pins should have dedicated and short paths to this pin.

7.3.1.3 VS (Voltage-Sense)

The VS pin is connected to a resistor divider from the auxiliary winding to ground. The output-voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. Timing information to achieve valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. The VS input is a critical signal and will generally be with relatively high impedance. To avoid unpredictable behavior avoid placing a filter capacitor on this pin and keep the total PCB area tied to VS at a minimum.

The VS pin also senses the bulk capacitor input voltage to provide for ac-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. This information is sensed by monitoring the current pulled out of the VS pin during the MOSFET on-time. During this time the voltage on the VS pin is clamped to about 250mV below GND. As a result, the current out of the pin is determined by the upper VS divider resistor, the auxiliary to primary turns-ratio and the bulk input voltage level. For the AC-input run/stop function, the run threshold on VS is $I_{VSL(run)}$ (typical 220 µA) and the stop threshold is $I_{VSL(stop)}$ (typical 80 µA). The values for the auxiliary voltage divider upper-resistor R_{S1} and lower-resistor R_{S2} can be determined by the equations below.

$$R_{S1} = \frac{\sqrt{2} \times V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \approx \frac{V_{BULK(run)}}{N_{PA} \times I_{VSL(run)}} \quad (1)$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio,
- $V_{IN(run)}$ is the AC rms voltage to enable turn-on of the flyback converter (run),
- $V_{BULK(run)}$ is the DC bulk voltage to enable turn-on of the flyback converter (run),
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the primary MOSFET on-time. (see the *Electrical Characteristics* table).

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \quad (2)$$

where

- V_{OCV} is the converter regulated output voltage,
- V_F is the output rectifier forward voltage drop at near-zero current,
- N_{AS} is the transformer auxiliary to secondary turns ratio,
- R_{S1} is the VS divider high-side resistance,
- V_{VSR} is the CV regulating level at the VS input (see the *Electrical Characteristics* table).

This pin is also used to sense the output constant current under voltage (CCUV) level, used to shut down the converter in the case of a soft-short circuit at its output. Refer to Constant Current Under-Voltage Protection for further information.

Feature Description (接下页)

7.3.1.4 DRV (Gate Drive)

The DRV pin is connected to the MOSFET gate pin, usually through a series resistor. The DRV provides a gate drive signal which is clamped to 10.5-V internally. During turn-on the driver applies a typical 30-mA current source out of the DRV pin. When the DRV voltage rises to above 9 V the output current is reduced to about 100 µA. This current brings the DRV voltage to the 10.5-V clamp level, or to VDD, whichever is less. The 30-mA current provides adequate turn-on speed while automatically limiting noise generated at turn-on by the MOSFET drain dv/dt and by the leading edge turn-on current spike. The gate drive turn-off current is internally limited to about 400 mA when DRV is above about 4 V. At lower DRV voltages the current will reduce, eventually being limited by the low-side on resistance, $R_{DS(on)}$. The drain turn-on and turn-off dv/dt can be further impacted by adding external resistor in series with DRV pin. The drain current resonances can be damped with a small series gate resistor, generally less than a 1 Ω.

7.3.1.5 CS (Current Sense)

The current sense pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The controller varies the internal current sense threshold between 0.188 V and 0.75 V, setting a corresponding control range for the peak-primary winding current to a 4-to-1 range. The series resistor R_{LC} provides an input voltage feed-forward function. The voltage drop across this resistor reduces primary-side peak current as the line voltage increases, compensating for the increased di/dt and delays in the MOSFET turn-off. There is an internal leading-edge blanking time of 255 ns to eliminate sensitivity to the MOSFET turn-on leading edge current spike. If additional blanking time is needed, a small bypass capacitor, up to 30 pF, can be placed on between CS pin and GND pin. The value of R_{CS} is determined by the target output current in constant current (CC) regulation. The values of R_{CS} and R_{LC} can be determined by the equations below. The term η_{XFMR} is intended to account for the energy stored in the transformer but not delivered to the secondary. This includes transformer core and copper losses, bias power, and primary leakage inductance losses.

Example: With a transformer core and copper losses of 3%, leakage inductance caused power losses 2%, and bias power to output power ratio of 0.5%. The transformer power transfer efficiency is estimated as η_{XFMR} = 100% - 3% - 2% - 0.5% = 94.5%

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (3)$$

where

- V_{CCR} is a current regulation constant (see the *Electrical Characteristics* table),
- N_{PS} is the transformer primary-to-secondary turns ratio (a typical turns-ratio of 12 to 15 is recommended for 5-V output),
- I_{OCC} is the target output current in constant-current regulation,
- η_{XFMR} is the transformer efficiency.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times (t_D + t_{GATE\_OFF}) \times N_{PA}}{L_P} \quad (4)$$

where

- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- t_D is the current-sense delay (typical 50 ns) plus MOSFET turn-off delay,
- t_{GATE_OFF} is the primary-side main MOSFET turn-off time,
- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant (see the *Electrical Characteristics* table).

Feature Description (接下页)

7.3.1.6 NTC/SU (NTC Thermistor Shutdown and External Start Up Control)

The UCC28704 uses an external NTC resistor tied to the NTC/SU pin to program a thermal shutdown temperature for the power supply. The NTC/SU shutdown threshold is 0.95 V with an internal 105-µA current source which results in a 9.05-kΩ thermistor shutdown threshold. A small capacitor with value not greater than 100 pF can be used on this pin for any noise reduction purposes. The capacitor with its value greater than 100 pF can cause a false over-temperature protection response. The NTC/SU pin should be left floating if not used.

The NTC/SU pin can be used to control an external depletion-mode FET to enable active high-voltage start up, Refer to Initial Power-On with A Depletion-Mode FET for more detail.

7.3.2 Primary-Side Regulation (PSR)

图 12 illustrates a simplified flyback convertor with the main voltage regulation blocks of the device shown. The power train operation is the same as any DCM flyback circuit but accurate output voltage and current sensing is the key to primary-side control.

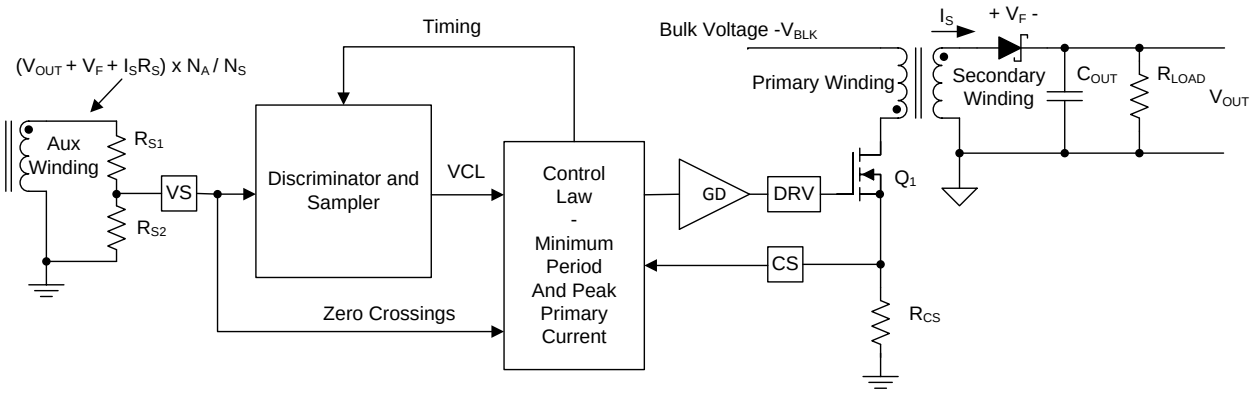


图 12. Simplified Flyback Convertor (with the Main Voltage Regulation Blocks)

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. As shown in 图 13 during this time, the auxiliary winding voltage has a down slope representing a decreasing total rectifier forward voltage drop V_F and resistance voltage drop ($I_S R_S$) as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.06 V; the resistor divider is selected as outlined in the VS pin description.

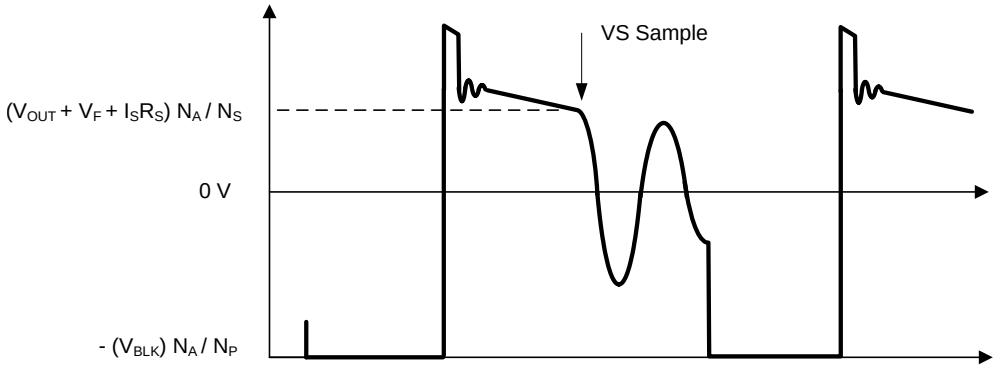


图 13. Auxiliary Winding Voltage

Feature Description (接下页)

The UCC28704 VS signal sampler includes signal discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. There are however critical details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring. Refer to 图 14 for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin. The first detail to examine is the duration of the leakage inductance reset pedestal, T_{LK_RESET} in 图 14. Since this can mimic the waveform of the secondary current decay, followed by a sharp downslope, it is important to keep the leakage reset time less than 750 ns for I_{PRI} minimum, and less than 3.0 µs for I_{PRI} maximum. The second detail is the amplitude of ringing on the V_{AUX} waveform following t_{LK_RESET}. The peak-to-peak voltage at the VS pin should be less than approximately 250 mV_{p-p} at least 250 ns before the end of the demagnetization time, t_{DMAG}. If there is a concern with excessive ringing, it usually occurs during light or no load conditions, when t_{DMAG} is at the minimum, $t_{DMAG(min)}$. The tolerable ripple on VS is scaled up to the auxiliary winding voltage by R_{S1} and R_{S2}, and is equal to 250 mV × (R_{S1}+R_{S2}) / R_{S2}. The snubber designs can be designed to allow the ripple voltage to meeting these requirements.

As mentioned in Device Functional Modes, when $I_{PP} < I_{PP(max)}$, the device operation enters a “Wait” state during each switching cycle of its non-switching portion as shown in 图 14. In the *Wait* state, the device bias current changes to I_{WAIT} (typical 70 µA) from I_{RUN} (typical 2.3 mA), reducing its bias power to help boost efficiency at light load and to reduce standby load power.

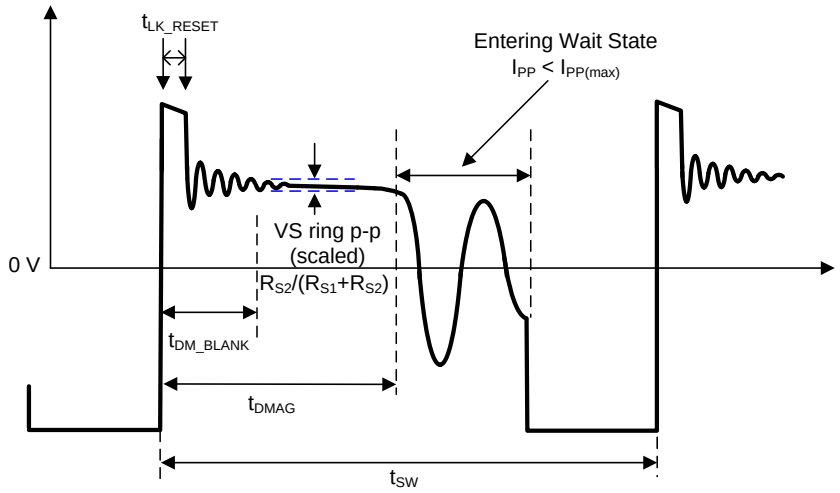


图 14. Auxiliary Waveform Details

Feature Description (接下页)

7.3.3 Primary-Side Constant Voltage (CV) Regulation

During voltage regulation (CV mode), the controller operates in frequency modulation mode and peak current amplitude modulation mode as illustrated in 图 15 below. The UCC28704 incorporates internal voltage-loop compensation circuits so that external compensation is not necessary, provided that the value of C_{OUT} is high enough. The following equation determines a minimum value of C_{OUT} necessary to maintain a phase margin of about 40 degrees over the full-load range,

$$C_{OUT} \geq 100 \times \frac{I_{OCC}}{V_{OCV} \times f_{MAX}} \tag{5}$$

The internal operating frequency limits of the device are $f_{SW(max)}$ and $f_{SW(min)}$, typically 85 kHz and 1 kHz, respectively. The choice of transformer primary inductance and primary-peak current sets the maximum operating frequency of the converter, which must be equal to or lower than $f_{SW(max)}$. Conversely, the choice of maximum target operating frequency and primary-peak current determines the transformer primary-inductance value. The actual minimum switching frequency for any particular converter depends on several factors, including minimum loading level, leakage inductance losses, switch-node capacitance losses, other switching and conduction losses, and bias-supply requirements. In any case, the minimum steady-state frequency of the converter must always exceed $f_{SW(min)}$ or the output voltage may rise to the over-voltage protection level (OVP) and the controller responds as described in Fault Protection.

To achieve a regulated output voltage in the CV mode operation, energy balance has to be maintained. As the UCC28704 has a minimum switching frequency typical 1 kHz, together with the energy per switching cycle determined by converter parameters, such as the transformer primary inductance Lp and the selected R_{CS} resistor, the converter has a minimum input power. A proper pre-load needs to be selected to ensure that this minimum energy is balanced during the no-load condition. The selection of the line compensation resistor value (R_{LC}) connected to the CS pin can impact the energy per switching cycle based on low-line and high-line conditions. Typical Application section provides a design example to show how to implement these considerations.

In the CV mode operation, the cable compensation is in effect. The cable compensation is to adjust the output voltage at board-end to be higher than the no-load setup point, noted as V_{OCV}, then to compensate the voltage drop due to the cable resistance through which the load current I_O is flowing. The UCC28704 cable compensation is fixed at 6% of V_{OCV} at full load, and the board-end output voltage is described by 公式 6:

$$V_{OUT} = V_{OCV} \times (1 + 0.06 \times \frac{I_O}{I_{OCC}}) \tag{6}$$

Feature Description (接下页)

Due to the cable compensation, the output voltage at board-end is seen higher than V_{OCV} with a positive slope when load current I_O> 0. The output voltage at the cable's end can be flat, upturned, or downturned, depending on the cable total resistance in use. Primary-Side Constant Current (CC) Regulation has more descriptions on the cable compensation.

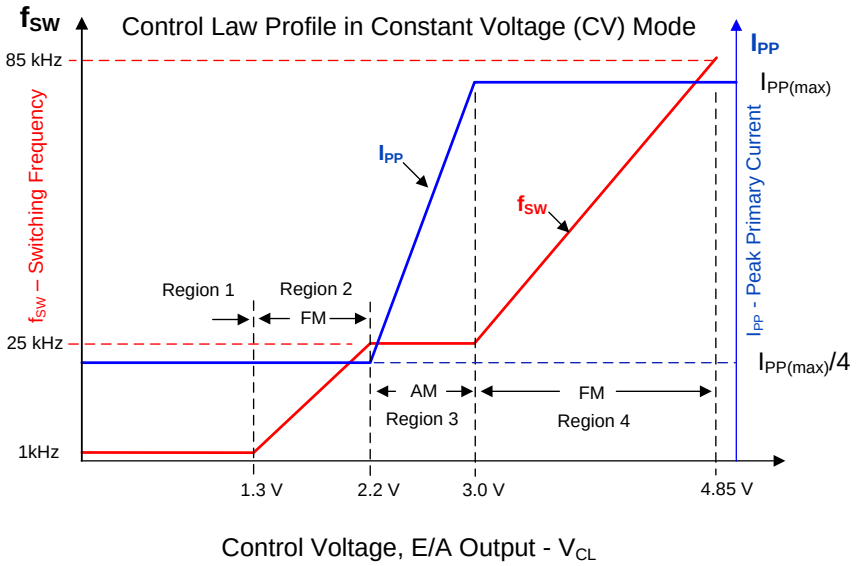


图 15. Frequency and Amplitude Modulation Modes (during CV mode)

In CV mode operation, the control consists of four regions, namely, region 1 through 4. The device internal error op-amp output V_{CL} sets a particular region operation. Refer to 图 12 for V_{CL}. The steady-state control-law voltage, V_{CL}, ranges between 1.3 V to 4.85 V. Heavy load operation is usually in region 4 where frequency modulation to output regulation is used and primary-peak current is controlled at its maximum. Region 3 is usually for medium-load range typically from 10% load and above. In this region switching frequency is fixed at nominal 25 kHz along with primary-peak current varying from 25% to 100% of its maximum. A low operating frequency range (region 2) is for lighter loads to achieve stable regulation at low frequencies. In region 2, peak-primary current is always maintained at $I_{PP(max)}/4$ in the lower frequency level. Transitions between levels are automatically accomplished by the controller depending on the internal control-law voltage, V_{CL}. During a load transient condition when V_{CL} > 4.85 V, the device operates in constant current mode. When load is in step-down transient demanding frequency lower than 4 kHz, first, the device stays at 4 kHz for up to 500 ms, or the output voltage reaches about 10% over the V_{OCV} within 500 ms, then the device adjusts the switching frequency to be lower than 4 kHz as needed. More details can be found in Load Transient Response.

Feature Description (接下页)

7.3.4 Primary-Side Constant Current (CC) Regulation

Timing information at the VS pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary-peak current is at $I_{PP(max)}$. Referring to 图 16 below, the primary peak current (I_{PP}), turns-ratio (N_S/N_P), secondary demagnetization time (t_{DMAG}), and switching period (t_{SW}) determine the secondary average output current. Ignoring leakage inductance effects, the average output current is given by 公式 7. By regulating the secondary rectifier conduction duty cycle, the output average current is constant for given I_{PP} and transformer turns-ratio. When the load increases, the secondary-side rectifier conduction duty cycle keep increasing. Once it reaches preset value of 0.475, the converter switching frequency is then reduced to maintain 0.475 secondary-side duty cycle. Therefore, the output current is kept constant. Because the current is kept constant, the increasing load results in lower output voltage. Converter can shut down in this condition if the output voltage drops below CCUV protection level, or UCC28704 VDD drops below its UVLO turn-off threshold.

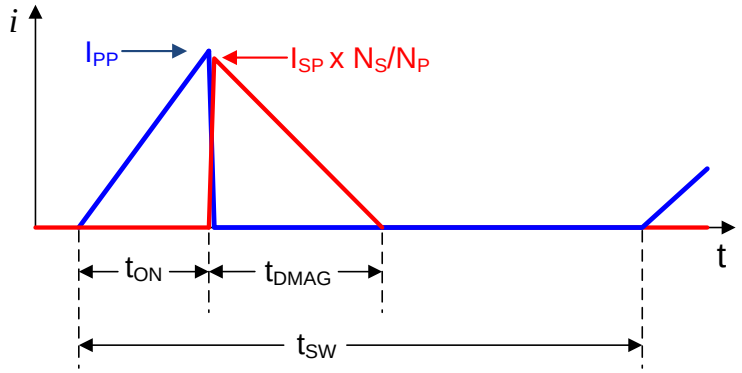


图 16. Transformer Currents

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DMAG}}{t_{SW}} \quad (7)$$

As shown in 图 17 below, CV mode operation is from I_O = 0 to I_{OCC}; at $I_O = I_{OCC}$, the operation enters CC mode and V_O starts to drop as the load resistance becomes further lower while I_O is maintained at I_{OCC} until Vo reaches the CCUV threshold. Details of the CCUV operation are given in Constant Current Under-Voltage Protection. 图 17 shows the output at board-end and at cable-end. The cable compensation nominally compensates 300 mV for a 5V-output at the I_{OCC} level.

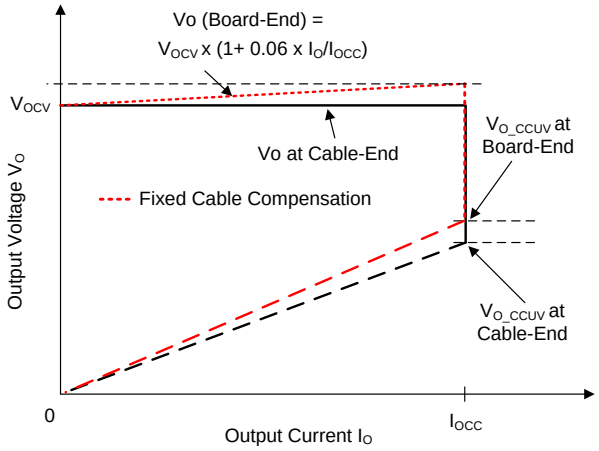


图 17. Typical Target Output V-I Characteristic

Feature Description (接下页)

7.3.5 Valley-Switching and Valley-Skipping

The UCC28704 utilizes valley switching to reduce switching losses in the MOSFET, reduce induced-EMI, and minimize the turn-on current spike at the sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing diminished.

Referring to 图 18 below, the UCC28704 operates in a valley-skipping mode in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

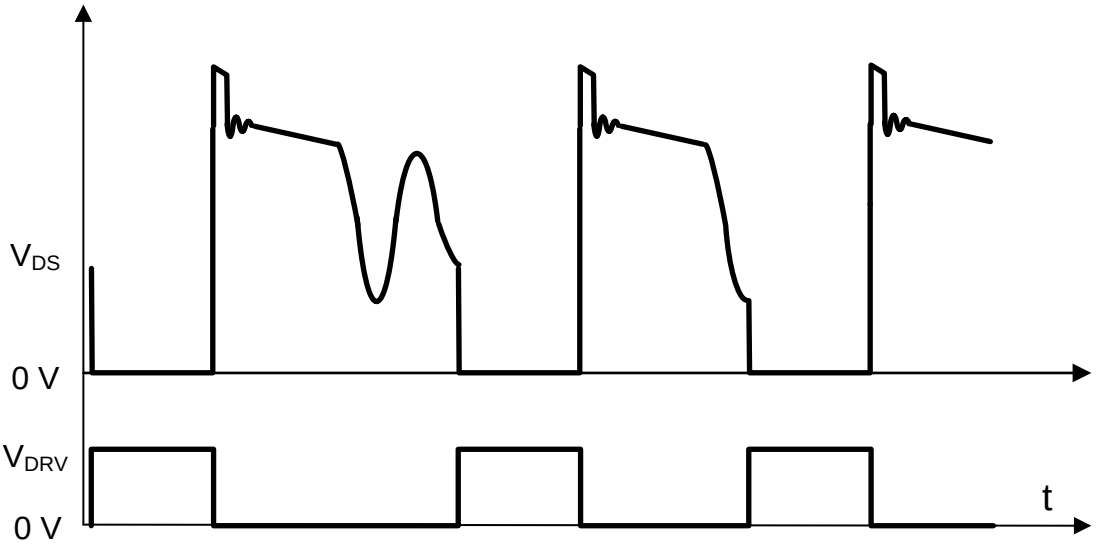


图 18. Valley-Skipping Mode

The UCC28704 forces a controlled minimum switching period corresponding to the power supply operating frequency. In each switching cycle, after the minimum period is expired, the UCC28704 looks for the next resonant valley on the auxiliary winding. The controller initiates a new power cycle at this valley point which corresponds to a reduced voltage level on the power MOSFET. If at the point in time when the minimum period expires ringing on the transformer winding has decayed such that no further resonant valleys can be detected a new power cycle is initiated following a fixed time, t_{ZTO}.

Feature Description (接下页)

7.3.6 Start-Up Operation

Upon application of input voltage to the converter, the start up resistance connected to VDD from the bulk capacitor voltage (V_{BULK}) charges the VDD capacitor. During charging of the VDD capacitor, the device supply current is less than 1.5 µA. When VDD reaches the 21-V UVLO turn-on threshold, the controller is enabled and the converter starts switching. The peak-primary currents with initial three cycles are limited to $I_{PP(min)}$. This allows sensing any initial input or output faults with minimal power delivery. When confirmed that the input voltage is above the programmed converter turn-on voltage and with no faults detected, the start-up process proceeds and normal power conversion follows. The converter remains in discontinuous conduction mode operation during charging of the output capacitor(s), maintaining a constant output current until the output voltage is in regulation.

Initial power-on to the UCC28704 device is achieved by one of the two approaches that are described in Initial Power-On with a Start-Up Resistor and Initial Power-On with A Depletion-Mode FET.

7.3.6.1 Initial Power-On with a Start-Up Resistor

A common used initial power-on approach for UCC28704 is to use a start-up resistor, R_{STR}, to tie VDD to V_{BLK}, as show in 图 19. With this approach, the VDD pin is connected to a bypass capacitor to ground and a start-up resistance to the input bulk capacitor (+) terminal. The VDD turn-on UVLO threshold is 21 V ($V_{VDD(on)}$)and turn-off UVLO threshold is 7.7 V ($V_{VDD(off)}$), with an available operating range up to 35 V. The USB charging practice requires the output current to operate in constant-current mode from 5 V to typical about 3 V; this is easily achieved with a nominal VDD of approximately 15 V. The additional VDD headroom up to 35 V allows for VDD to rise due to the leakage energy delivered to the VDD capacitor in high-load conditions. Also, the wide VDD range provides the advantage of selecting a relatively small VDD capacitor and high-value start-up resistance to minimize no-load stand-by power loss in the start-up resistor.

The R_{STR} value has effect to power-on delay time and no-load standby power losses. Both are usually part of the design specifications. Increase R_{STR} reduces standby power losses while increases power-on delay time. A typical range of R_{STR} is from 10 MΩ to 15 MΩ as initial design start point for off-line AC-to-DC adapters where power-on delay time usually requires less than two seconds. Due to the limited voltage rating, R_{STR} is normally implemented by two or three resistors in series.

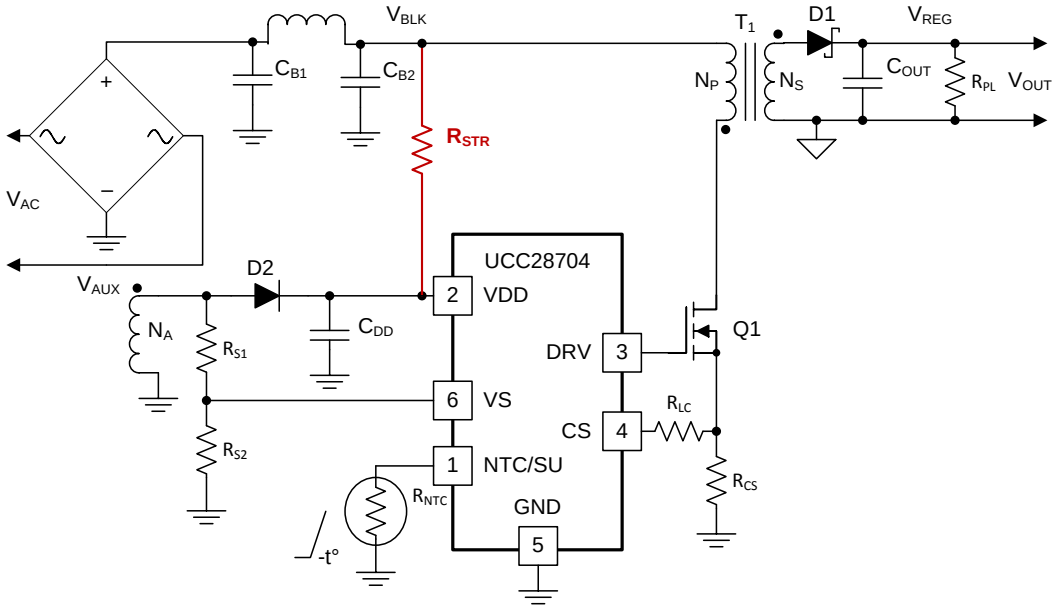


图 19. Power-On with Start-Up Resistor

Feature Description (接下页)

7.3.6.2 Initial Power-On with A Depletion-Mode FET

The UCC28704 NTC/SU pin can control an external depletion-mode FET to provide more efficient start-up. This provides a fast start-up time with eliminating the loss associated with the start-up circuit. Therefore, the standby power at no load can be minimized. This gives an alternative method to power on the device initially. As shown in 图 20, the depletion mode FET HV start-up circuit consists of Q_{ST1}, Q_{ST2}, C_{ST}, R_{ILIM}, and R_{ST1} to R_{ST3}.

Before VDD reaches $V_{VDD(on)}$, NTC/SU stays low, Q_{ST1} turns on, which enables the quick charge of C_{DD} thereby achieving a shorter power-on delay time. After VDD ≥ $V_{VDD(on)}$, NTC/SU starts sourcing 105 µA to turn on Q_{ST2} then turns off Q_{ST1}. This stops Q_{ST1} providing current to UCC28704 and minimizes the loss in the start-up circuit. In normal operation when $I_{PP} < I_{PP(max)}$, the device enters *wait* state in each switching cycle, see 图 14 for *wait* state time. During *wait* state, NTC/SU stops sourcing 105 µA; which turns off Q_{ST2} and can potentially cause Q_{ST1} to turn on. Hence C_{ST} is added to ensure that Q_{ST1} is off even during *wait* state. For reference, R_{ST1} = R_{ST2} = 2 MΩ, R_{ST3} = 100 kΩ, C_{ST} = 1 nF, R_{ILIM} = 365 kΩ, as an example. To select a depletion-mode FET for Q_{ST1}, BSS126 or similar can be an option.

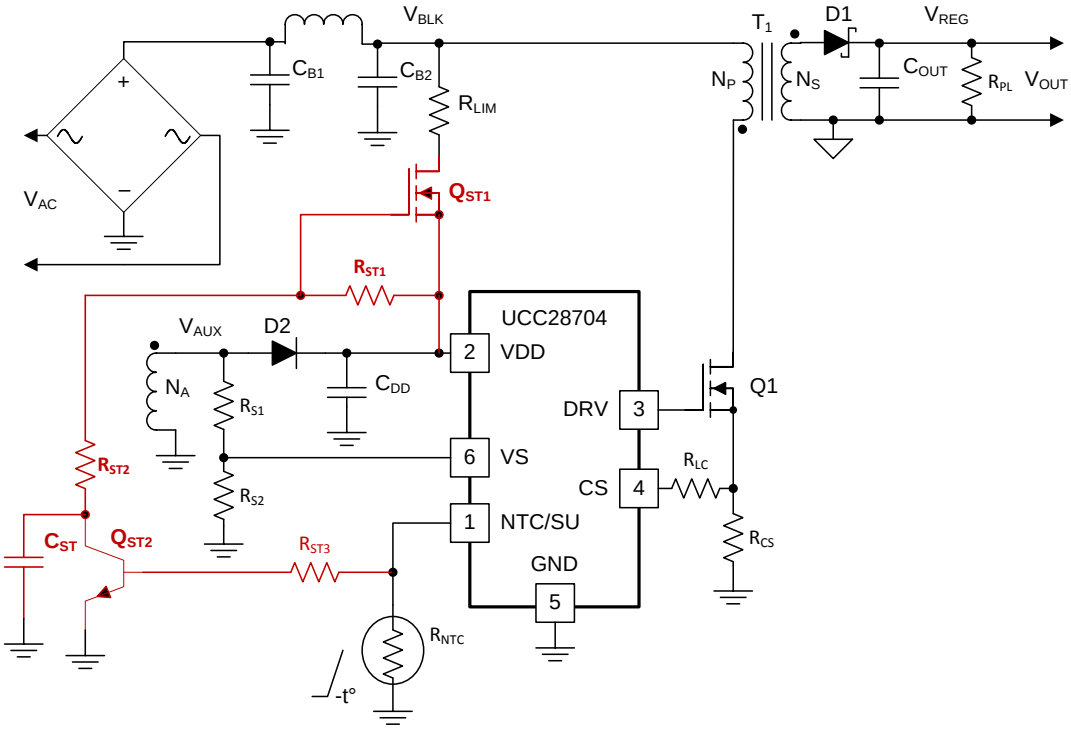


图 20. Power-On with a Depletion-Mode FET

Feature Description (接下页)

7.3.7 Fault Protection

There is comprehensive fault protection incorporated into the UCC28704. Protection functions include:

- Output Over-Voltage
- Input Under-Voltage
- Primary Over-Current Fault
- CS Pin Open Fault
- CS Pin Short-to-GND Fault
- VS Pin Fault
- External NTC Over-Temperature
- Device Internal Over-Temperature
- Constant Current Under Voltage Output Shutdown (CCUV) for Soft-Short Protection

Output Over-Voltage: The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 4.67 V, 115% of the nominal regulating level, for three consecutive switching cycles an OV fault is asserted. Once asserted the device stops switching, initiating a UVLO reset and re-start fault cycle. During the fault, the VDD bias current remains at the run current level, discharging the VDD pin to the UVLO turn-off threshold, $V_{VDD(off)}$. After that, the device returns to the start state, VDD now charging to $V_{VDD(on)}$ where switching is initiated. The UVLO sequence repeats as long as the fault condition persists.

Input Under-Voltage: The line input run and stop thresholds are determined by current information at the VS pin during the MOSFET on-time. While the VS pin is clamped close to GND during the MOSFET on-time, the current through R_{S1}, out of the VS pin, is monitored to determine a sample of the bulk capacitor voltage. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage. From the start state, the sensed VS current, I_{VSL}, must exceed the run current threshold, $I_{VSL(run)}$ (typical 220 µA), within the first three cycles after switching starts as VDD reaches $V_{VDD(on)}$. If it does not, then switching stops and the UVLO reset and re-start fault cycle is initiated. Once running, I_{VSL} must drop below the stop level, $I_{VSL(stop)}$ (typically 80 µA), for three consecutive cycles to initiate the fault response.

Primary Over-Current: The UCC28704 always operates with cycle-by-cycle primary-peak current control. The normal operating range of the CS pin is 0.75 V to 0.188 V. If the voltage on CS exceeds the 1.5-V over-current level, any time after the internal leading edge blanking time and before the end of the transformer demagnetization, for three consecutive cycles the device shuts down and the UVLO reset and re-start fault cycle begins.

CS Pin Open: The CS pin has a 2-µA minimum pull-up that brings the CS pin above the 1.5-V OC fault level if the CS pin is open. This causes the primary over-current fault after three cycles.

CS Pin Short to GND: On the first, and only the first cycle at start-up, the device checks to verify that the $V_{CST(min)}$ threshold is reached at the CS pin within 4 µs of DRV going high. If the CS voltage fails to reach this level then the device terminates the current cycle and immediately enters the UVLO reset and re-start fault sequence.

VS Pin: Protection is included in the event of component failures on the VS pin. If the high-side VS divider resistor opens the controller stops switching. VDD collapses to its $V_{VDD(off)}$ threshold, a start-up attempt follows with a single DRV on-time when VDD reaches $V_{VDD(on)}$. The UVLO cycle will repeat. If the low-side VS divider resistor is open then an output over-voltage fault occurs.

NTC Over-Temperature: UCC28704 uses the NTC/SU pin to program thermal shutdown threshold with an external NTC thermistor on this pin. The NTC shutdown threshold is 0.95 V with an internal 105-µA current source which results in a 9.05-kΩ thermistor shutdown threshold. If the NTC/SU pin voltage is below 0.95 V at the end of the secondary current demagnetization time for three consecutive cycles switching stops and the UVLO reset and re-start fault sequence is initiated.

Device Internal OTP: The internal over-temperature protection threshold is 150°C. If the junction temperature of the device reaches this threshold the device initiates the UVLO reset and re-start fault cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Constant Current Under-Voltage: Output shutdown (CCUV) for soft-short protection. Constant Current Under-Voltage Protection provides detailed description for this fault and fault response.

Feature Description (接下页)

7.3.8 Constant Current Under-Voltage Protection

The constant current output under voltage shutdown (CCUV) feature is to provide protection for USB connectors from over-heat or burn-out due to soft-short circuit fault. A partial or soft-short can happen due to the presence of foreign objects at the terminals of the USB upstream facing port, UFP, for example, smartphones with USB Micro-B or USB Type-C connectors. When this happens along with the converter operates in CC mode with enough VDD voltage (VDD > $V_{VDD(off)}$) available from auxiliary winding, the converter can sustain operation at this condition resulting in a potential USB burn-out condition which is named as *soft-short* fault to distinguish from a *hard-short* circuit fault. Traditional over-current protection and short-circuit protection cannot tell a soft-short fault. The UCC28704 provides protection when soft-short circuit fault occurs with the corresponding converter V-I characteristics as shown in 图 21.

As shown in 图 22, the CCUV feature of UCC28704 detects the operation of the converter under this condition when the controller is operating in CC mode and when the output voltage drops out of regulation, reaching the CCUV threshold. If the controller detects that the VS pin voltage is below V_{CCUV} threshold continuously for 120 ms, then it initiates a CCUV fault and sets the CCUV latch. Once the CCUV latch is set, the controller goes through 3 cycles of VDD-UVLO without any PWM operation and clears the latch on the 4th VDD UVLO power-up. If the CCUV condition still exists, then the controller enters into CCUV fault after 120 ms and repeats the UVLO cycles. This 120-ms time delay allows converter normal start up without triggering the CCUV protection. The flyback design should allow output voltage rise above CCUV protection level under normal operating conditions within 120ms or the CCUV fault may be triggered.

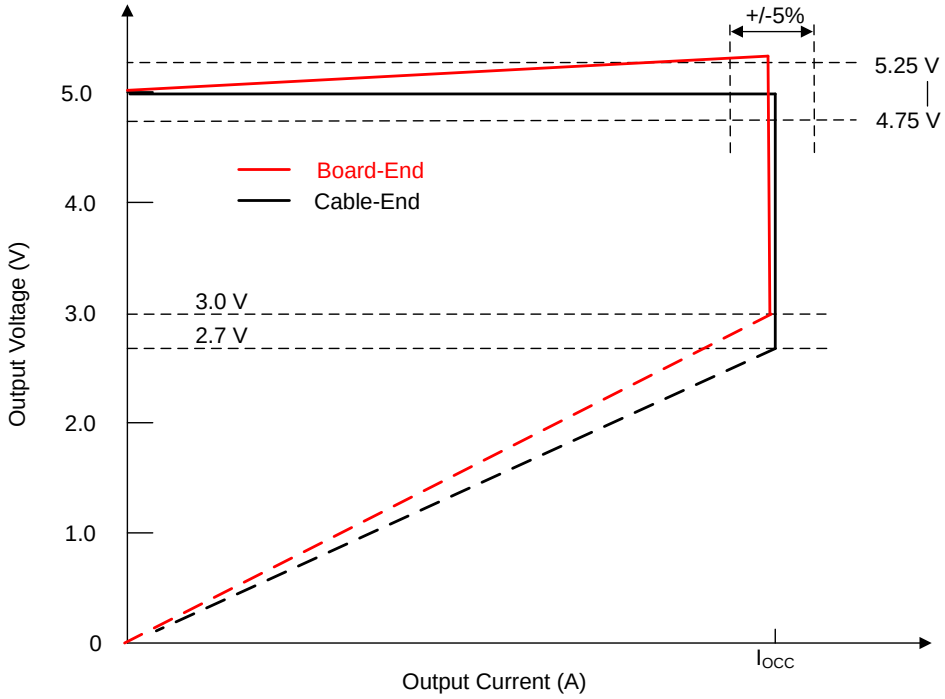


图 21. Typical Target Output V-I Curves

Feature Description (接下页)

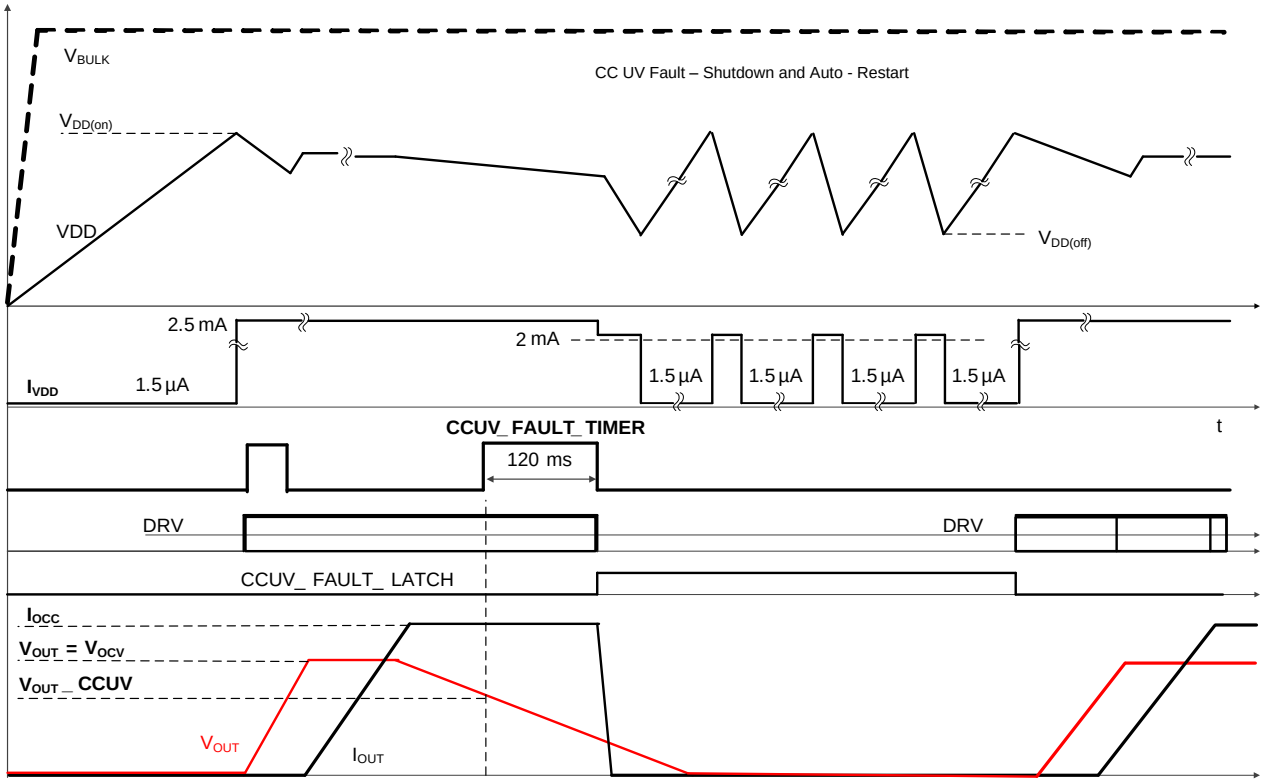


图 22. Timing Diagram of CCUV and Output Re-Start

Feature Description (接下页)

7.3.9 Load Transient Response

The UCC28704 can provide excellent transient performance for most load steps. However the response of PSR controller is always limited by the operating frequency of the converter, since the controller only samples or reads the output voltage once every switching cycle. At zero external load, or standby, the operating frequency is set by any preload together with the bias power needed. This frequency, $f_{SW(standby)}$, sets a maximum incremental response delay. The preload can always be adjusted, at the expense of standby power, to increase the standby frequency. The actual response delay depends on the relative timing of the load step within the switching cycle. Thus for a given load step, $I_{OUT(step)}$, the output deviation can be as large as:

$$\Delta V_{OUT} = \frac{I_{OUT(step)}}{C_{OUT} \times f_{SW(standby)}} \quad (8)$$

In the case of repeating load transients the situation is aggravated. Whenever the load steps from a modest current level to zero, there is a period of time when there is a slight over-shoot in the output voltage and the control loop saturates and force the converter operating at to its minimum switching frequency, $f_{SW(min)}$, or 1 kHz regardless what preload setting is. If the next positive load step occurs during this time the output deviation will be larger, remembering that $f_{SW(standby)}$ must be > $f_{SW(min)}$.

A special transient response algorithm in this controller dynamically adjusts the minimum controlled switching frequency, such that during a mid to high current level condition the loop's minimum switching frequency is raised to $f_{SW(lim)}$, typically 4 kHz. This raised minimum switching frequency is maintained following a load step-down change until the output voltage rises momentarily to 10% above its normal regulating level or has stayed above its normal regulating level for 500 ms. During this time the response to a load step-up change benefits from the decreased response delay afforded by the 4-kHz switching frequency. This is illustrated in 图 23. Application Curves provides test results and further description in regarding to this technique.

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In applications where standby power is not critical the minimum operating frequency of the loop can be kept higher than 4 kHz. In these cases controller will continuously maintain a 4-kHz minimum frequency.

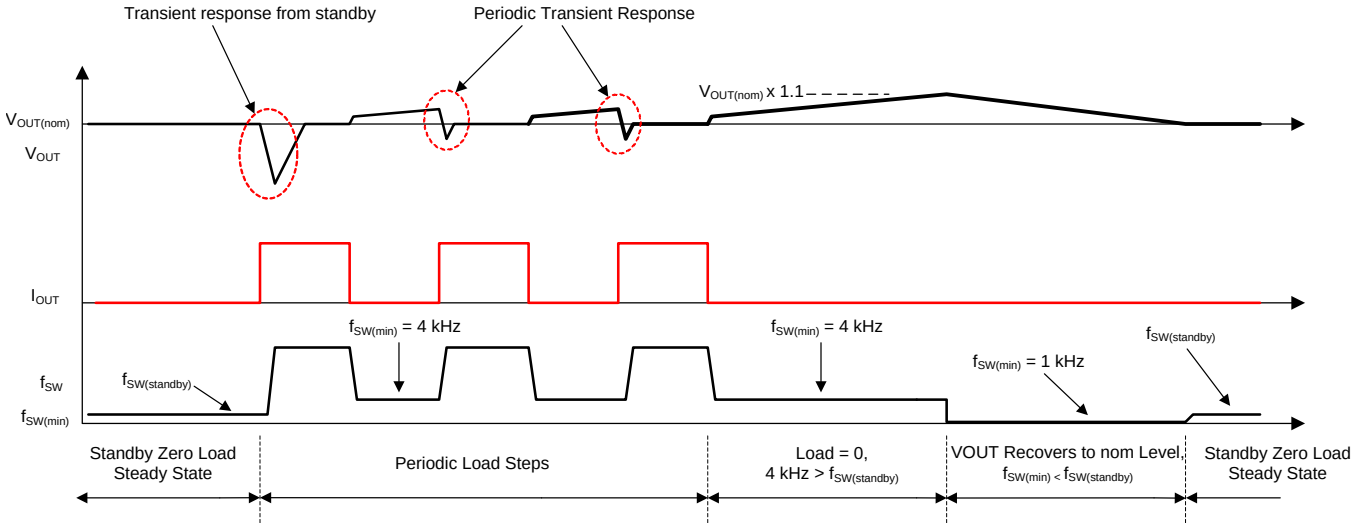

图 23. Dynamic Load Response

7.4 Device Functional Modes

The UCC28704 operates in different modes according to input voltage, VDD voltage, and output load conditions:

- At start-up, when VDD is less than the turn-on threshold, $V_{VDD(on)}$, the device is simply waiting for VDD to reach this threshold while the VDD capacitor is getting charged.
- When VDD exceeds $V_{VDD(on)}$, the device starts switching to deliver power to the converter output. The initial 3 switching cycles control the primary-peak current to $I_{PP(min)}$. This allows sensing any initial input or output faults with minimal power delivery. When confirmed with input voltage above predetermined level and no fault conditions, start up process proceeds and normal power conversion follows. The converter will remain in discontinuous current mode operation during charging of the output capacitor(s), maintaining a constant output current until the output voltage reaches its regulation point.
  - CV mode means that the converter keeps the output voltage constant. When the load current is less than the current limit level, the converter operates in CV mode to keep the output voltage at the regulation level over the entire load and input line ranges.
  - CC mode means that the converter keeps the output current constant. When the output voltage is below the regulation level, the converter operates in CC mode to limit the output current.
  - In CC mode, when the output voltage starts to drop below regulation and if it reaches below the CCUV threshold V_{CCUV}, sensed at the VS pin, the controller declares a CCUV fault and disables PWM. The controller initiates a shutdown-restart operation. This protection mode helps avoid USB terminals from getting over-heated and thereby preventing a burn-out condition, which is also called soft-short protection. Detailed description is in Constant Current Under-Voltage Protection.
- When operating in CV mode where I_{PP} reaches $I_{PP(max)}$, the UCC28704 operates continuously in the *run* state. In this state, the VDD bias current is always at I_{RUN} plus the average gate-drive current.
- When operating in CV mode where I_{PP} is less than $I_{PP(max)}$, the UCC28704 operates in the *wait* state between switching cycles and in the *run* state during a switching cycle. In the *wait* state, the VDD bias current is reduced to I_{WAIT} after demagnetizing time of each switching cycle to improve efficiency at light loads. This helps reduce light-load power losses, particularly for achieving higher efficiency at 10% and 25% load conditions.
- When a dynamic load change occurs in CV mode, the UCC28704 provides an enhanced transient response to reduce load step caused V_{OUT} dip in periodic load change operation. Detailed description is in Load Transient Response.
- The device operation can be stopped by the events listed below:
  - If VDD drops below the $V_{VDD(off)}$ threshold, the device stops switching, its bias current consumption is lowered to I_{START} until VDD rises above the $V_{VDD(on)}$ threshold. The device then resumes switching.
  - If a fault condition is detected, the device stops switching and its bias current consumption becomes I_{FAULT}. This current level discharges VDD to $V_{VDD(off)}$ where the bias current changes from I_{FAULT} to I_{START} until VDD rises above the $V_{VDD(on)}$ threshold.
  - By pulling down NTC/SU pin to below V_{NTCTH}, the device responds similar to that of an NTC fault wherein PWM is disabled and converter is shutdown. On releasing the pull-down on NTC, normal operation into CV mode will be restored.
- If a fault condition persists, the operation sequence described above in repeats until the fault condition or the input voltage is removed. Refer to Fault Protection for fault conditions and post-fault operation.

8 Applications and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC28704 device is a PSR controller optimized for isolated-flyback AC-to-DC single-output supply applications, typically in the range from 5 W to 25 W, providing constant-voltage (CV) mode control and constant current (CC) mode control for precise output regulation; and to help meet USB-compliant adaptors and charger requirements as well as help meeting DOE Level VI or CoC V5 Tier 2 efficiency performance. The device uses the information obtained from auxiliary winding sensing (VS) to control the output voltage without requiring optocoupler/TL431 feedback circuitry. Not requiring optocoupler feedback reduces the component count and makes the design more cost effective.

8.2 Typical Application

图 24 illustrates a typical circuit diagram for AC-to-DC adapter applications. It is a flyback converter with primary-side regulation (PSR) controlled by UCC28704. Such applications widely exist in ac-dc adapters for smartphones, tablet-computers, and e-readers and so forth. The following sub-sections provide critical design formulas.

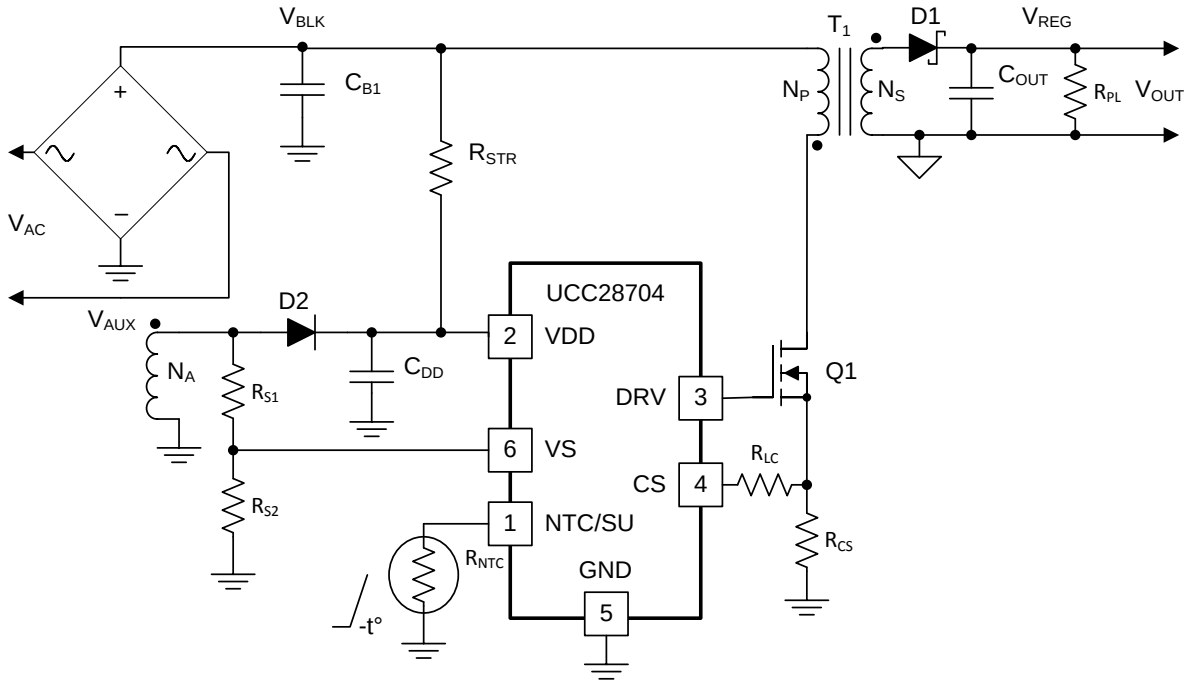


图 24. Typical Application Circuit

Typical Application (接下页)

8.2.1 Design Requirements

The following table illustrates a typical subset of high-level design requirements for a particular converter of which many of the parameter values are used in the various design equations in this section. Many other necessary design parameters, such as $f_{SW(MAX)}$ and $V_{BULK(min)}$ for example, may not be listed in such a table. These values may be selected based on design experience or other considerations, and may be iterated to obtain optimal results.

表 1. UCC28704 Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	AC-line input voltage		85	115/230	265	V_{RMS}
f_{LINE}	Line frequency		47	50/60	63	Hz
P_{STBY}	No-load input power	V_{IN} = typ, I_O = 0A		43	50	mW
OUTPUT CHARACTERISTICS (MEASUREMENT AT 150-mΩ CABLE-END)						
V_O	DC output voltage	V_{IN} = typ, I_O = 0 to I_{OR}	4.75	5	5.25	V
V_{RIPPLE}	Output voltage ripple	V_{IN} = typ, I_O = I_{OR}			80	mV
I_{OR}	Output rated current	V_{IN} = min to max		2.0		A
I_{OCC}	Output constant current	V_{IN} = typ, I_O > I_{OR} 2.7V < V_O < 5V	2.1	2.2	2.3	A
V_{CCUV}	CC UV shutdown interception	V_{IN}= typ, I_O = I_{OCC}		2.7		V
η_{AVG}	Average efficiency	V_{IN}= typ, average of 25%, 50%, 75%, and 100% Load	80%			
η_{10}	Light-load efficiency	V_{IN}= typ, 10% load	75%			
SYSTEMS CHARACTERISTICS						
f_{sw}	Switching frequency		1		65	kHz
$T_{ON-Delay}$	Power-on delay time	V_{IN} = min I_O= I_{OR} (constant resistor load)			1.8	s

8.2.2 Detailed Design Procedure

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28704 controller. Please refer to the 图 24 for circuit details and section *器件命名规则* for variable definitions used in the applications equations below.

8.2.2.1 VDD Capacitance, C_{DD}

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage. At this time the auxiliary winding can sustain the voltage to the UCC28704. The total output current available to the load and to charge the output capacitors is the constant-current regulation target. The equation below assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage V_{OCC} is achieved. The gate-drive current depends on particular MOSFET to be used. If with an estimated 1.0 mA of gate-drive current, C_{DD} is determined by 公式 9.

$$C_{DD} = \frac{\left(I_{RUN} + 1.0mA\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{\left(V_{DD(on),min} - V_{DD(off),max}\right)} \tag{9}$$

8.2.2.2 VDD Start-Up Resistance, R_{STR}

Once the VDD capacitance is known, the start-up resistance from V_{BULK} to achieve the power-on delay time (t_{STR}) target can be determined.

$$R_{STR} = \frac{\sqrt{2} \times V_{IN(min)}}{I_{START} + \frac{V_{DD(on)} \times C_{DD}}{t_{STR}}} \tag{10}$$

8.2.2.3 Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input capacitance, C_{B1} and C_{B2} total, in order to determine the maximum Np to Ns turns ratio of the transformer. The input power of the converter based on target full-load efficiency, minimum input rms voltage, and minimum AC input frequency are used to determine the input capacitance requirement.

Maximum input power is determined based on V_{OCV}, I_{OCC}, and the full-load efficiency target. An initial estimate of 84% can be assumed for the full-load efficiency for a 5-V/2-A design.

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} \tag{11}$$

公式 12 provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage. To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{P_{IN} \times \left(0.5 + \frac{1}{\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2V_{IN(min)}^2 - V_{BULK(min)}^2\right) \times f_{LINE}} \tag{12}$$

8.2.2.4 Transformer Turns Ratio, Inductance, Primary-Peak Current

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM resonant time.

Initially determine the maximum available total duty cycle of the on time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if you do not have an estimate from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period, or 1 µs assuming 500-kHz resonant frequency. D_{MAX} can be determined using 公式 13.

$$D_{MAX} = 1 - \left(\frac{t_R}{2} \times f_{MAX} \right) - D_{MAGCC} \tag{13}$$

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with the equation below. D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant-current, CC, operation. It is set internally by the UCC28704 at 0.475. The total voltage on the secondary winding needs to be determined; which is the sum of V_{OCV}, the secondary rectifier V_F, and the cable compensation voltage (V_{OCBC}). For the 5-V USB charger applications, a turns ratio range of 12 to 15 is typically used for a 10-W design.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times \left(V_{OCV} + V_F + V_{OCBC} \right)} \tag{14}$$

N_{PS} is determined also with other design factors such as primary MOSFET, secondary rectifier diode, as well as secondary MOSFET if synchronous rectifier is used. Once an optimum turns-ratio is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28704 controller constant-current regulation is achieved by maintaining D_{MAGCC} = 0.475 at the maximum primary current setting. The transformer turns ratio and constant-current regulating voltage determine the current sense resistor for a target constant current limit.

Since not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power. For a 5-V, 2-A charger example, bias power of 0.5% is a good estimate. An overall transformer efficiency of 94.5% is a good estimation of assuming 2% leakage inductance, 3% core and winding loss, and 0.5% bias power.

R_{CS} is used to program the primary-peak current with 公式 15:

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \tag{15}$$

The primary transformer inductance can be calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output and transformer efficiency are included in 公式 16. Initially determine transformer primary current.

Initially the transformer primary current should be determined. Primary current is simply the maximum current sense threshold divided by the current sense resistance.

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \tag{16}$$

$$L_P = \frac{2 \times \left(V_{OCV} + V_F + V_{OCBC} \right) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \tag{17}$$

The secondary winding to auxiliary winding transformer turns ratio (N_{AS}) is determined by the lowest target operating output voltage in constant-current regulation and the VDD UVLO of the UCC28704. There is additional energy supplied to VDD from the transformer leakage inductance energy which allows a lower turns ratio to be used in many designs. The V_{OCC} lower than CCUV level is not achievable because the CCUV protection is going to be triggered first.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} \tag{18}$$

8.2.2.5 Transformer Parameter Verification

The transformer turns-ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage so these should be reviewed. The UCC28704 controller requires a minimum on time of the MOSFET (t_{ON}) and minimum D_{MAG} time ($t_{DMAG(min)}$) of the secondary rectifier in the high line, minimum-load condition. The selection of f_{MAX}, L_P and R_{CS} affects the minimum t_{ON} and t_{DMAG}.

The secondary rectifier and MOSFET voltage stress can be determined by the equations below.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \tag{19}$$

For the MOSFET V_{DS} voltage stress, an estimated leakage inductance voltage spike (V_{LK}) needs to be included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \tag{20}$$

The following equations are used to determine for the minimum t_{ON} target of 0.3 µs and minimum de-mag time, $t_{DMAG(min)}$, target of 1.7 µs. The minimum $t_{DMAG(min)}$ target needs to be typically 2.45 µs when a synchronous rectifier is used on the secondary-side instead of a Schottky diode rectifier. Additional details are provided in Design Considerations in Using with Synchronous Rectifiers.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \tag{21}$$

$$t_{DMAG(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \tag{22}$$

8.2.2.6 VS Resistor Divider, Line Compensation, and NTC

The VS divider resistors determine the output voltage regulation point of the flyback converter, also the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on the transformer auxiliary to primary turns-ratio and the desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \tag{23}$$

The low-side VS pin resistor is selected based on desired V_O regulation voltage. $I_{VSL(run)}$ is VS pin run current with a typical value 220 µA for a design.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times \left(V_{OCV} + V_F\right) - V_{VSR}} \tag{24}$$

The UCC28704 can maintain tight constant-current regulation over input line by utilizing the line compensation feature. The line compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and expected gate drive and MOSFET turn-off delay. Assume a 50-ns internal delay in the UCC28704.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times (t_D + t_{GATE\_OFF}) \times N_{PA}}{L_P} \tag{25}$$

The NTC function on NTC/SU-pin is to program with a NTC resistor for the desired over-temperature shutdown threshold. The shut-down threshold is 0.95 V with an internal 105-µA current source which results in a 9.05-kΩ thermistor shut-down threshold. The SU function on NTC/SU-pin is described in Initial Power-On with A Depletion-Mode FET. Pulling down this pin to GND stops switching and can be used for remote enable and disable control. This pin should be left floating if not used.

8.2.2.7 Standby Power Estimate

Assuming no-load standby power is a critical design parameter, determine the estimated no-load power based on target converter maximum switching frequency and output power rating. The following equation estimates the stand-by power of the converter.

$$P_{SB\_CONV} \cong \frac{P_{OUT} \times f_{MIN}}{\eta \times K_{AM}^2 \times f_{MAX}} \tag{26}$$

For a typical USB charger application, the bias power during no-load is approximately 2.1 mW. This is based on 21-V VDD and 100-µA bias current. The output preload resistor can be estimated by V_{OCV} and the difference in the converter stand-by power and the bias power. The equation for output preload resistance accounts for bias power estimated at 2.1 mW. Preload resistor value is estimated in 公式 27 :

$$R_{PL} = \frac{V_{OCV}^2}{P_{SB\_CONV} - 2.1mW} \tag{27}$$

Typical start-up resistance values for R_{STR} range from 10 MΩ to 15 MΩ to achieve less than 2-s start-up time. The capacitor bulk voltage for the loss estimation is the highest voltage for the stand-by power measurement, typically 325 V_{DC}.

$$P_{RSTR} = \frac{(V_{BULK} - V_{DD})^2}{R_{STR}} \tag{28}$$

For the total stand-by power estimation add an estimated 2.5 mW for snubber loss to the start-up resistance and converter stand-by power loss.

$$P_{SB} = P_{SB\_CONV} + P_{RSTR} + P_{SNBR} \tag{29}$$

8.2.2.8 Output Capacitance

The output capacitance value is typically determined by the transient response requirement from no-load. For example, in some USB charger applications there is a requirement to maintain a minimum V_O of 4.1 V with a load-step transient of 0 mA to 500 mA . 公式 30 assumes that the switching frequency can be at the UCC28704 minimum of $f_{SW(min)}$.

$$C_{OUT} = \frac{I_{TRAN}\left(\frac{1}{f_{SW(min)}} + 50\mu s\right)}{\Delta V_O} \tag{30}$$

公式 5 should be observed together with 公式 30 for stability consideration when determine C_{OUT}.

Another consideration of the output capacitor(s) is the ripple voltage requirement. The output capacitors and their total ESR are the main factors to determine the output voltage ripple. 公式 31 provides a formula to determine required ESR value R_{ESR}, and 公式 31 provides a formula to determine required capacitance. The total output ripple is the sum of these two parts with scale factors and 10mV to consider other noise as shown in 公式 33,

$$R_{ESR} = \frac{1}{I_{PP(max)} \times N_{PS}} \times V_{RIPPLE\_R} \tag{31}$$

$$C_{OUT} = \frac{L_P \times I_{PP(max)}^2}{4 \times (V_{OCV} + V_{CBC})} \times \frac{1}{V_{RIPPLE\_C}} \tag{32}$$

$$V_{RIPPLE} = 0.81 \times V_{RIPPLE\_R} + 1.15 \times V_{RIPPLE\_C} + 10mV \tag{33}$$

Example: if require V_{RIPPLE} = 70 mV, assume 0.81 × V_{RIPPLE_R} = 1.15 × V_{RIPPLE_C} = 30 mV, then R_{ESR} = 4.05 mΩ, and C_{OUT} = 643 µF, with assumption of L_P = 700 µH, $I_{PP(max)}$ = 0.713 A, N_{PS} = 13, V_{OCV} = 5 V, V_{CBC} = 0.3 V.

8.2.2.9 Design Considerations in Using with Synchronous Rectifiers

Special design considerations need to be observed when using synchronous rectifiers (SR) with the UCC28704. 图 14 depicts the de-mag time partition. When using UCC28704 with SR, a portion of the de-mag time needs to be reserved for t_{bw}, as shown in 图 25, which is the body diode conduction time when SR MOSFET turns off before the de-mag time ends.

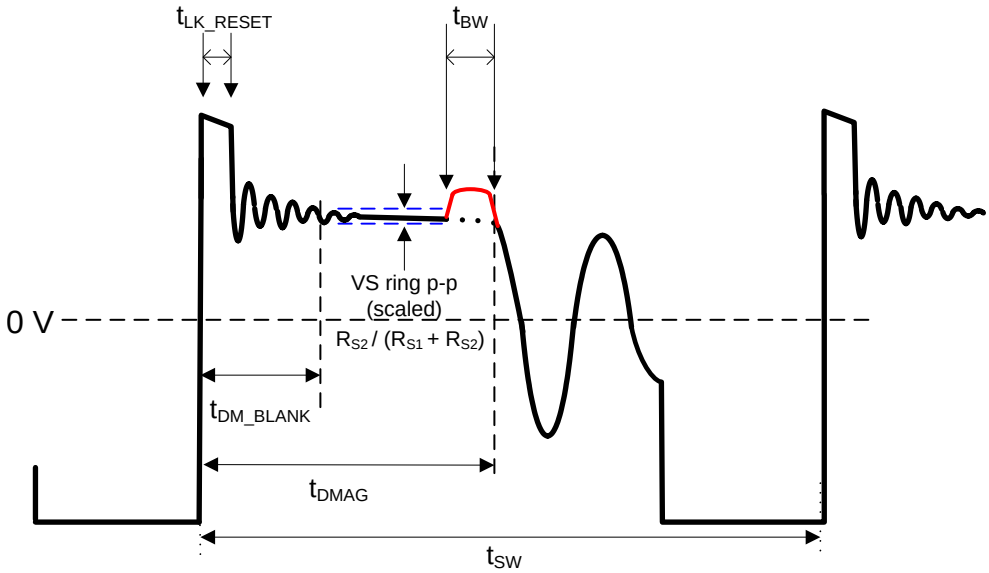


图 25. Auxiliary Waveform Details

The critical parameter dictating the maximum switching frequency when UCC28704 is used with an SR is determined based on $t_{DMAG(min)}$. The $t_{DMAG(min)}$ needs to be typically 2.45 µs including the SR bump width (t_{BW}) is 750 ns. The 750-ns (t_{BW}) is required for the internal circuit to filter out the SR bump change caused by MOSFET body diode conduction that is sensed on the VS pin waveform. The corresponding switching frequency measured at starting point of constant current operation should not be greater than 55 kHz.

8.2.3 Application Curves

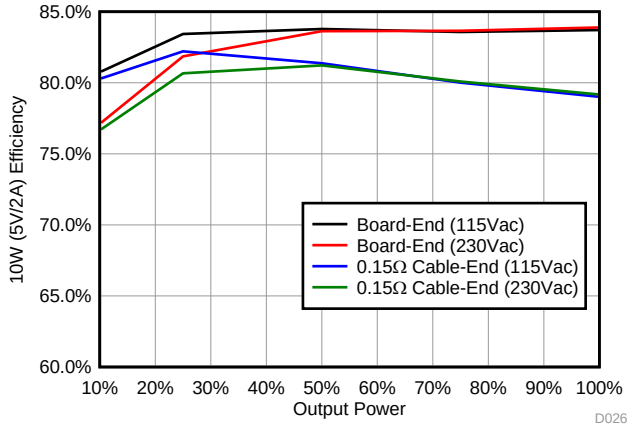


图 26. Efficiency

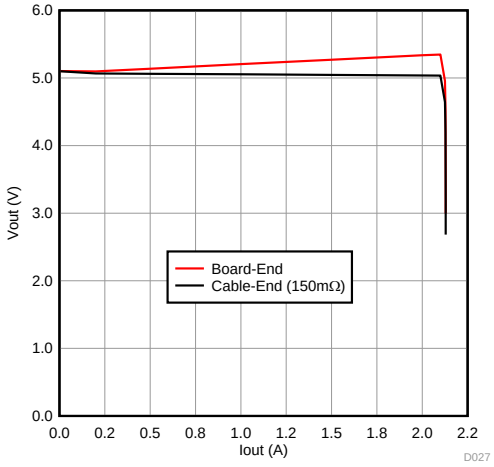


图 27. Output V-I Curves

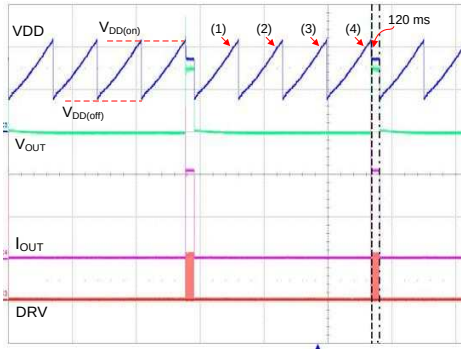


图 28. Soft-Short Protection

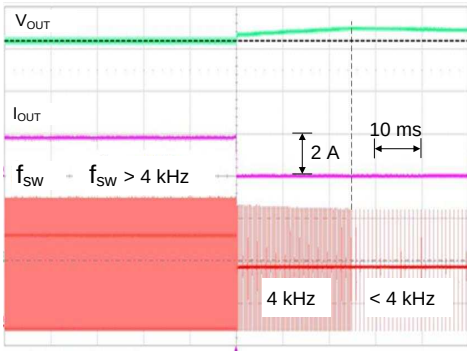


图 29. Response to Load Step-Down

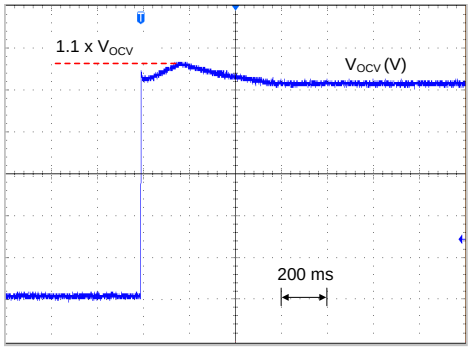


图 30. Typical V_{OUT} Start Up at No Load

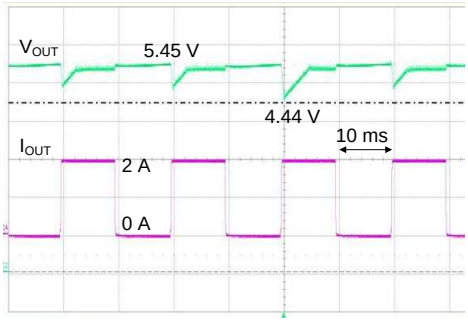


图 31. Typical Output Load Transient Response

图 26 shows efficiency test result based on a 5-V/2-A, 10-W adapter using UCC28704. The efficiency performance exceeds CoC V5 Tier 2 (79% for average and 69.7% for a 10%-load) and DOE Level VI (78.7% for average) measured at 150-mΩ cable-end. As comparison, the measured result at board-end shown in 图 26.

图 27 shows typical VI curves from the same 10-W board. The board-end output voltage has cable compensation to achieve cable-end output voltage with very well-regulated result in constant voltage mode operation range. In constant current mode operation, the result depicts a good constant current operation from the vertical line of current along with the output voltage drop until reaches CCUV. Notice that the CCUV difference at board-end and at cable-end is about 300 mV that is the same as cable compensation voltage at full load.

图 28 illustrates the timing diagram when the operation is in CCUV. The response of the controller to a soft-short circuit is shown wherein V_{OUT} reaches to less than the V_{CCUV} threshold. The converter is in CC mode and any additional load tending higher than I_{OCC} causes V_{OUT} to drop below regulation due to the soft-short. As V_{OUT} is able to sustain VDD above its UVLO and the soft-short circuit condition persists continuously for 120 ms, the CCUV fault is initiated. The waveform shows the 3 VDD UVLO cycles that the controller goes through after the fault and it attempts to restart on the 4th VDD UVLO cycle with the response repeating due to the sustained soft short-circuit fault. The 120 ms is to blank any possible noise interference which may cause unnecessary CCUV protection to interrupt a normal operation.

图 29 provides the test result to explain the enhanced load transient scheme that is described in Load Transient Response. When the load steps down and demands a lower switching frequency, the controller clamps the switching frequency at 4 kHz until either the output has gone above its regulation level for more than 500 ms or has reached more than 10% of its V_{OCV}. This enables the converter to have a better response to an ensuing load step up from the reduced response time. If either of the condition is met, then the controller starts to adjust the f_{SW} below 4 kHz if the converter operation demands such a frequency.

Associated to this enhancement, the output voltage may experience a 10% overshoot as shown in 图 29 during a load step-down or as shown in 图 30 during a no-load start up.

图 31 shows the output load transient with load step change between 0-A and 2-A full load.

8.3 Do's and Don'ts

- During no-load operation, do allow sufficient margin for variations in VDD level to avoid the UVLO shutdown threshold. Also, at no-load, keep the average switching frequency greater than 1.5 × $f_{SW(min)}$ typical to avoid a rise in output voltage. R_{LC} needs to be adjusted based on no-load operation accounting for both low-line and high-line operation..
- Do clean flux residue and contaminants from the PCB after assembly. Uncontrolled leakage current from VS to GND causes the output voltage to increase, while leakage current from VDD to VS can cause output voltage to increase.
- If ceramic capacitors are used for VDD, do use quality parts with X7R or X5R dielectric rated 50 V or higher to minimize reduction of capacitance due to DC-bias voltage and temperature variation.
- Do not use leaky components if low stand-by input power consumption is a design requirement.
- Do not probe the VS node with an ordinary oscilloscope probe; the probe capacitance can alter the signal and disrupt regulation.
- Do observe VS indirectly by probing the auxiliary winding voltage at R_{S1} and scaling the waveform by the VS divider ratio.
- Do follow 公式 5, 公式 30, 公式 31 to 公式 33 for C_{OUT}.

9 Power Supply Recommendations

The UCC28704 is intended for AC-to-DC adapters and chargers with universal input voltage range of 85 V_{RMS} to 265 V_{RMS}, 47 Hz to 63 Hz, using flyback topology. It can also be used in other applications and converter topologies with different input voltages. Be sure that all voltages and currents are within the recommended operating conditions and absolute maximum ratings of the device.

10 Layout

10.1 Layout Guidelines

In order to increase the reliability and feasibility of the project it is recommended to adhere to the following guidelines for PCB layout. In 图 32, a typical 5-V/2-A USB adapter design schematic is shown in 图 32.

- Minimize stray capacitance on the VS node. Place the voltage sense resistors (R_{S1} and R_{S2} in 图 24) close to the VS pin.
- Arrange the components to minimize the loop areas of the switching currents as much as possible. These areas include such loops as the transformer primary winding current loop (a), the MOSFET gate-drive loop (b), the primary snubber loop (c), the auxiliary winding loop (d) and the secondary output current loop (e). In practice, trade-offs may have to be made. Loops with higher current should be minimized with higher priority. As a rule of thumb, the priority goes from high to low as (a) – (e) – (c) – (d) – (b).
- The R_{LC} resistor location is critical. To avoid any dv/dt induced noise (for example MOSFET drain dv/dt) coupled onto this resistor, it is better to place R_{LC} closer to the controller and avoid nearby the MOSFET.
- To improve thermal performance increase the copper area connected to GND pins.

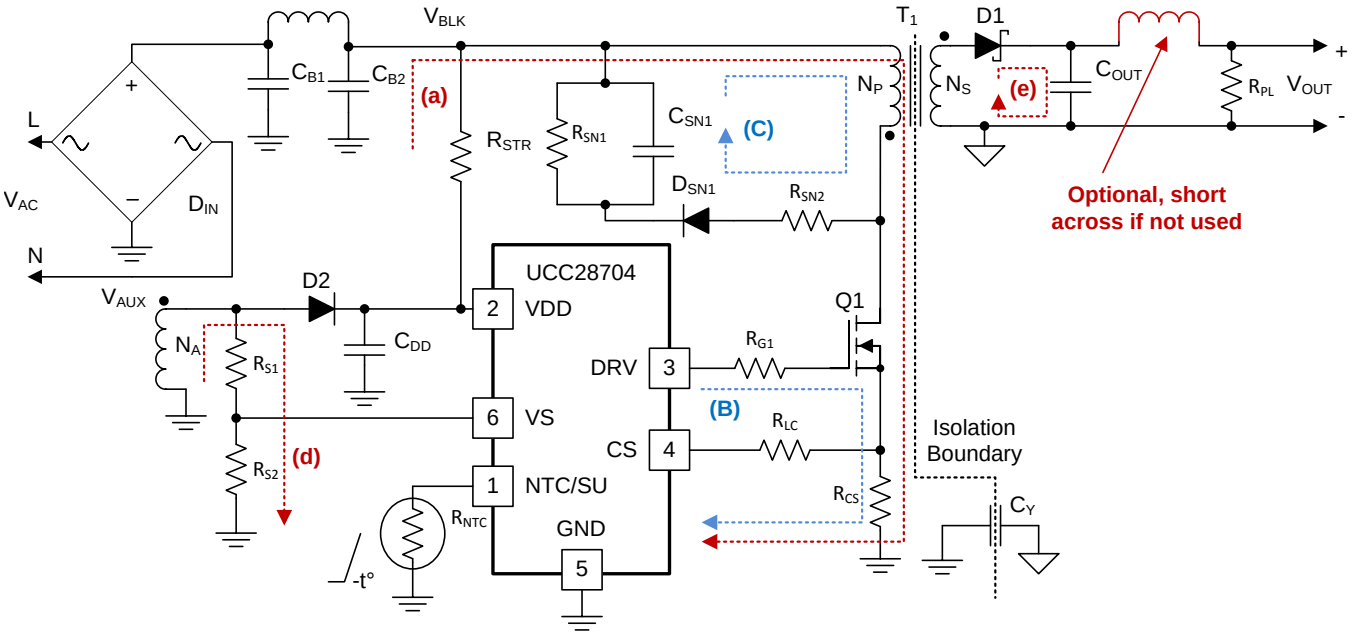


图 32. 10-W, 5-V/2-A USB Adapter Schematics

10.2 Layout Example

图 33 demonstrates a 10-W, 5-V/2-A, layout with trade-offs to minimize the loops while effectively placing components and tracks for low noise operation on a single-layer printed circuit board. In addition to the consideration of minimal loops, one another layout guideline is always to use the device GND as reference point. This applies to both power and signal to return to the device GND pin (pin 5).

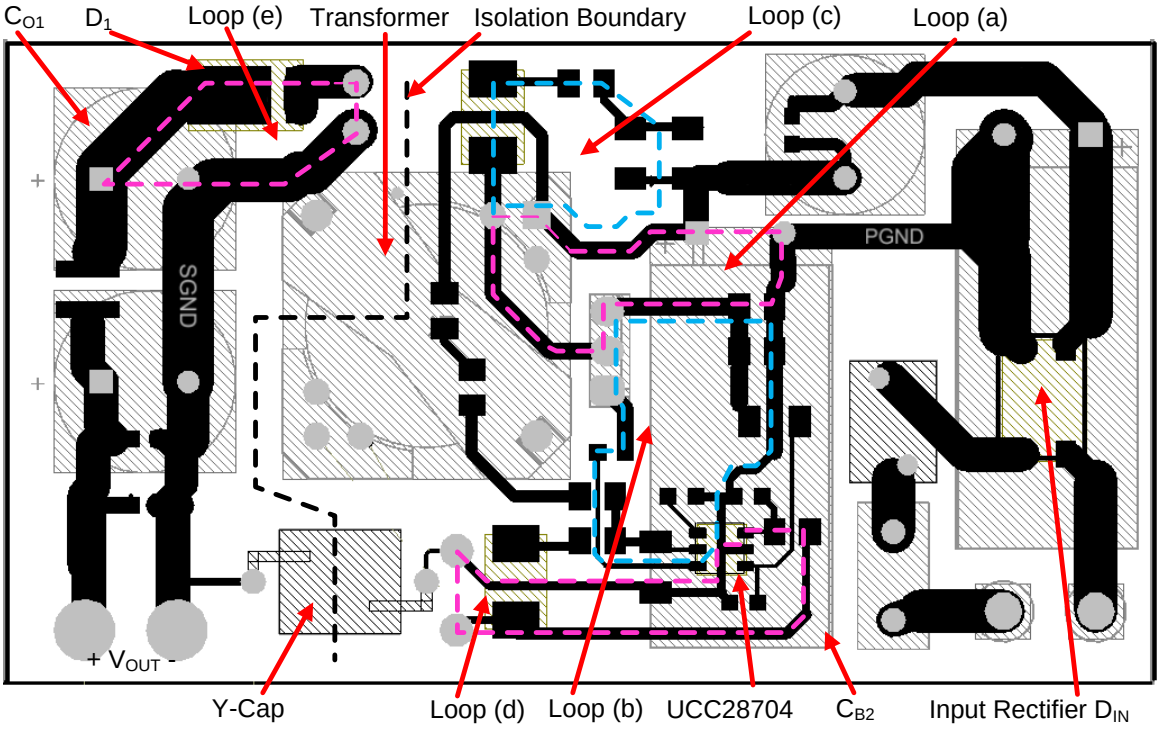


图 33. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

11.1.1.1 电容术语（以法拉为单位）

C_{BULK} C_{B1} 和 C_{B2} 的总输入电容。

C_{DD} VDD 引脚所需的最小电容。

C_{OUT} 所需的最小输出电容。

11.1.1.2 占空比术语

D_{MAGCC} CC 中二次侧二极管导通占空比，0.475。

D_{MAX} 最大 MOSFET 导通时间占空比。

11.1.1.3 频率术语（以赫兹为单位）

f_{LINE} 最低线路频率。

f_{MAX} 转换器的最高目标满载开关频率。

f_{MIN} 转换器的最低开关频率，在器件 $f_{SW(min)}$限值基础上增加 15% 的裕度。

$f_{SW(lim)}$ 负载减小后的瞬态开关频率

$F_{SW(min)}$ 最低开关频率（见*Electrical Characteristics*表）

$f_{SW(max)}$ 最大开关频率（见*Electrical Characteristics*表）

$f_{SW(standby)}$ 轻负载条件下负载变化之前的开关频率

11.1.1.4 电流术语（以安培为单位）

I_{OCC} 转换器输出恒流目标。

I_{OR} 转换器额定输出电流。

$I_{PP(max)}$ 变压器一次侧最大电流。

I_{START} 启动偏置电源电流（见*Electrical Characteristics*表）。

I_{TRAN} 所需的正负载阶跃电流。

$I_{VSL(run)}$ VS 引脚运行电流（见*Electrical Characteristics*表）。

I_{WAIT} 等待状态期间的 VDD 偏置电流。（见*Electrical Characteristics*表）。

11.1.1.5 电流和电压调节术语

K_{AM} 一次侧峰峰值电流比（见*Electrical Characteristics*表）。

K_{Co} 稳定性因子为 100，用于计算 C_{OUT}。

K_{LC} 电流调节常量（见*Electrical Characteristics*表）。

器件支持 (接下页)

11.1.1.6 变压器术语

L_P 变压器一次侧电感。

L_S 变压器二次侧电感。

N_{AS} 变压器辅助绕组与二次侧绕组匝数比。

N_{PA} 变压器一次侧绕组与辅助绕组匝数比。

N_{PS} 变压器一次侧绕组与二次侧绕组匝数比。

N_A 变压器辅助绕组的匝数。

N_P 变压器一次侧绕组的匝数。

N_S 变压器二次侧绕组的匝数。

11.1.1.7 功率术语（以瓦特为单位）

P_{IN} 转换器最大输入功率。

P_{OUT} 转换器的满载输出功率。

P_{RSTR} VDD 启动电阻功耗。

P_{SB} 总待机功耗。

P_{SB_CONV} P_{SB} 与启动电阻和缓冲器功耗的差值。

11.1.1.8 电阻术语（以 Ω 为单位）

R_{CS} 一次侧电流编程电阻

R_{ESR} 输出电容的总 ESR。

R_{PL} 转换器输出端的预载电阻。

R_{S1} 高侧 VS 引脚电阻。

R_{S2} 低侧 VS 引脚电阻。

R_{STR} 高电压与 VDD 之间连接的启动电阻

11.1.1.9 时序术语（以秒为单位）

t_D 电流感测延迟。

$t_{DMAG(min)}$ 二次侧整流器最短导通时间。

t_{GATE_OFF} 一次侧主 MOSFET 关断时间。

$t_{ON(min)}$ MOSFET 最短导通时间。

t_R t_{DMAG} 之后的谐振环周期。

t_{STR} 由于 VDD 电容 C_{DD} 需要充电时间所造成的上电延时。

t_{ZTO} tZTO：未检测到过零点时 VS 引脚上的过零点超时延迟（见*Electrical Characteristics*表）

器件支持 (接下页)

11.1.1.10 电压术语（以伏特为单位）

V_{BLK} 或 V_{BULK} 大容量电容电压。

$V_{BULK(max)}$ 用于待机功耗测量的大容量电容最高电压。

$V_{BULK(min)}$ 满功率条件下 C_{B1}和 C_{B2} 的最低电压。

$V_{BULK(run)}$ 转换器启动（运行）高电压。

V_{CBC} 满载时电路板端输出的电缆补偿电压。

V_{CCR} 恒流调节电压（见*Electrical Characteristics*表）。

V_{CCUV} 恒流输出电压关断的 VS 阈值（见*Electrical Characteristics*表）

$V_{CST(max)}$ CS 引脚的最大电流感测阈值（见*Electrical Characteristics*表）。

$V_{CST(min)}$ CS 引脚的最小电流感测阈值（见*Electrical Characteristics*表）。

$V_{VDD(off)}$ UVLO 关断电压（见*Electrical Characteristics*表）。

$V_{VDD(on)}$ UVLO 导通电压（见*Electrical Characteristics*表）。

V_F 电流接近零时的二次侧整流器正向压降。

V_{FA} 辅助整流器正向压降。

V_{LK} 估计的漏感能量复位电压。

V_{OCV} 经稳压的转换器输出电压。

V_{OCC} 恒流稳压条件下的最低目标转换器输出电压。

V_{RIPPLE} 满载条件下的输出峰峰值纹波电压。

V_{VSR} VS 输入端的 CV 调节电平（见*Electrical Characteristics*表）。

11.1.1.11 交流电压术语（以 V_{RMS} 为单位）

$V_{IN(max)}$ 转换器的最大输入电压。

$V_{IN(min)}$ 转换器的最小输入电压。

$V_{IN(run)}$ 转换器输入启动（运行）电压。

11.1.1.12 效率术语

η 转换器总体效率。

η_{10} 10% 负载时的效率。

η_{AVG} 25%、50%、75% 和 100% 负载时的算术平均效率。

η_{XFMR} 变压器一次侧与二次侧之间的功率传输效率。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

《使用 UCC28704-1EVM-724，评估模块》，SLUUBF1

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28704DBVR-1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7041	Samples
UCC28704DBVT-1	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7041	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

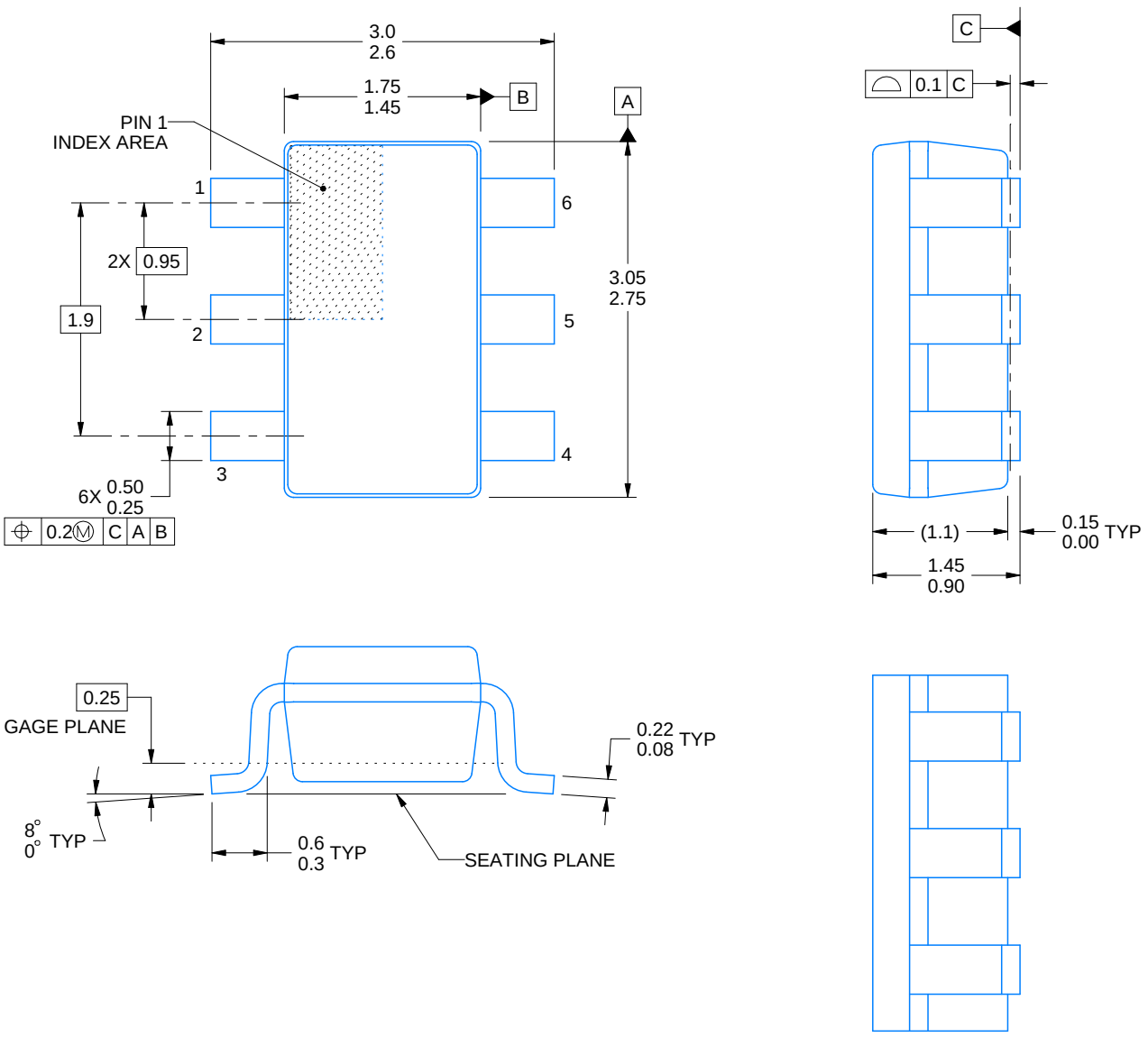
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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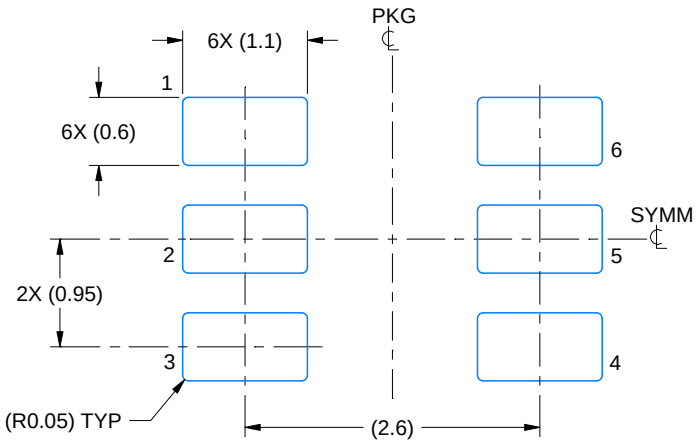
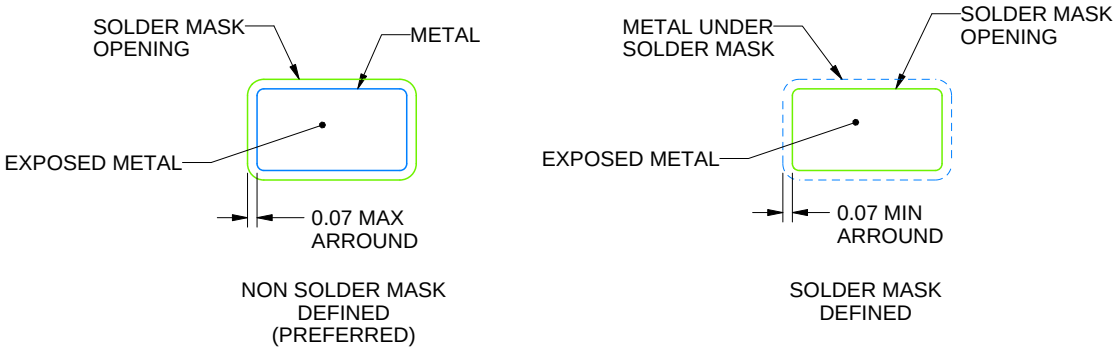
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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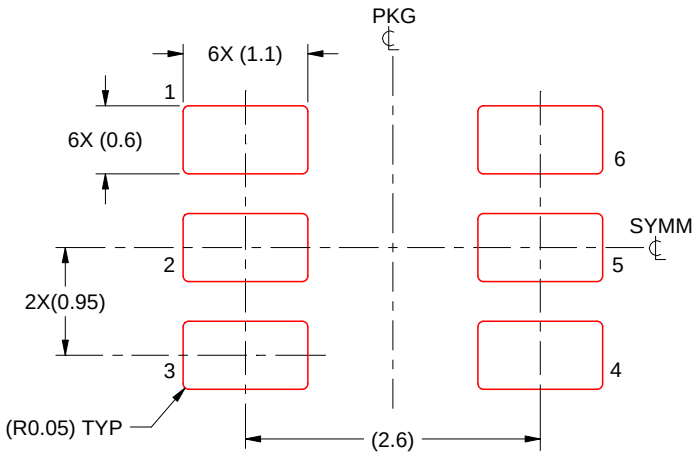
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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