Intel® Ethernet Controller I225/ I226

Datasheet

General

- Integrated MAC/PHY supporting 10BASE-Te,100BASE-TX, 1000BASE-T and 2500BASE-T 802.3 specifications
- IEEE 802.3u auto-negotiation conformance
- Carrier extension support (half duplex)
- Half duplex operation at 10BASE-Te and 100BASE-TX
- Automatic polarity correction
- Network proxy/ARP offload
- MDC/MDIO management interface
- Smart speed operation for automatic speed reduction on faulty cable plants
- Power optimizer support
- Intel® Stable Image Platform Program (SIPP)

Interconnects

- 1 lane PCIe Gen 2 v3.1 interface for active state operation
- SMBus interface to Intel vPro® engine at low system power state
- Integrated MDI termination resistors reducing BOM costs
- Configurable MDI TAP up/down operation
- Three configurable LED outputs

Package & Design

- 7x7 mm PG-VQFN-56 with a 0.4 mm lead pitch and an Exposed Pad* for ground
- Commercial temperature: 0 °C to +70 °C
- I225-IT Extended temperature:
  - 2.5G: -40 °C to +70 °C
  - 10M/100M/1G: -40 °C to +85 °C
- I226-IT Industrial temperature:
  - 10M/100M/1G/2.5G: -40 °C to +85 °C
- Integrated Switching Voltage Regulator (iSVR)

Advanced Features

- Error Correcting Memory (ECC) in packet buffers
- UDP, TCP and IP checksum offload
- UDP and TCP Transmit Segmentation Offload (TSO)
- SCTP receive and transmit integrity offload
- Queues: 4 Tx and 4 Rx queues
- PXE Support:
  - I225: Legacy PXE (minimal support) and EFI PXE
  - I226: EFI PXE only

Time Sensitive Networking (TSN) – FDX Network

- IEEE 1588 - Basic time-sync (Precision Time Protocol)
- IEEE 802.1AS-Rev - Higher precision time synchronization with multiple (dual) clock masters
- IEEE 802.1Qav - Credit Based Shaping and Basic scheduling
- IEEE 802.1Qbu - Frame Preemption
- IEEE 802.1Qbv - Time Aware Shaper
- IEEE 802.3br - Interspersing Express Traffic
- PCIe PTM for synchronization between the NIC and Host timers

Performance

- Four transmit and four receive queues
- Jumbo frames (up to 9 KB and without TSN)
- Receive Side Scaling (RSS) and MSI-X to lower CPU use in multi-core systems

Power

- IEEE 802.3az Energy Efficient Ethernet (EEE) – I226 only
- Ultra-low power at cable disconnected (18 mW) – I226 only
- Single-pin LAN disable for easier BIOS implementation
- Modern standby system support
- Advanced Configuration and Power Interface (ACPI) power management states and wake-up capability
- Advanced Power Management (APM) wake-up functionality
- Low power link up state
- PCIe v2.1 Latency Tolerance Reporting (LTR)
- PCIe v3.1 L1 sub-states
- DMA coalescing for improved system power management

Security & Manageability

- Authenticated Flash image
- Flash wear-out protection
- Intel® vPro support with appropriate Intel chipset
- MCTP over PCIe and over SMBus

Others

- For operating systems and SKU features breakdown, refer to the I225/226 Message of the Week (MOW)

Revision 2.6
February 2022

Revision History

Revision	Date	Comments
2.6	February 2022	Update table 1-1, table 1-6, chapter 1.2, 3.6, 3.6.1, 4.1 Update 7.2.2 Recommended Operating Conditions
2.5.2	November 2021	Update the media type on chapter 8.7
2.5.1	November 2021	Update the description on pin 34 and pin 37 in table 2-5
2.5	October 2021	Adding I226 Added Device ID Table Updated Power Consumption Table Updated Default SMBUS Slave Address Updated image for figure 3-1 NMV Structure
2.0	October 2020	Updated title page. Changed industrial temperature information to extended temperature. Updated Ethernet media interface. Added note for SMBus resistor pull-up value. Added default SMBus slave address. Added general power state information. Updated BOM list (to support extended temperature applications). Updated order information. Added new section (2.7.1; Leakage Avoidance on LAN Power Disconnect).
1.92	March 2020	Updated title page (commercial/industrial temp values). Revised table 7.2.2 (recommended operating conditions).
1.91	March 2020	Initial Release.

1.0 Introduction

The Intel® 2.5 Gigabit Ethernet Controller I225/I226 is a single-port, compact, low power Gigabit Ethernet (GbE) controller. It is a fully integrated GbE Media Access Control (MAC) and Physical Layer (PHY) device, offering 10/100/1000/2500 Mb/s data rates. The interface-to-host system is a one lane PCI Express* (PCIe*) Gen 2 (5.0GT/s) version 3.1.

Note: I225 v1 (B1 stepping) reaches 2.5 GbE on select switches/routers. Refer to the *Intel® Ethernet Controller I225 Public External Specification Update* for more detail.

1.1 Feature Summary

The I225/I226 enables 2.5 GbE BASE-T implementations using an integrated MAC/PHT architecture. It can be used for client systems, server systems and dock configurations such as desktop, laptops, workstations, server, Thunderbolt™ dock in add-on Network Interface Card (NIC) or LAN on Motherboard (LOM) designs.

The I225/I226 is packaged in a small footprint VQFN package. Package size is 7 x 7 mm with a 0.4 mm lead pitch and a height of 0.85 mm, making it very attractive for small form-factor platforms.

The I225/I226 supports the Intel vPro®. The interface to the vPro® engine is over SMBus as well as the PCIe link at active system state.

The I225/I226 also supports a Time Sensitive Network (TSN) that can be used in Audio/Video Bridging (AVB) applications and extended temperature applications that require TSN capabilities.

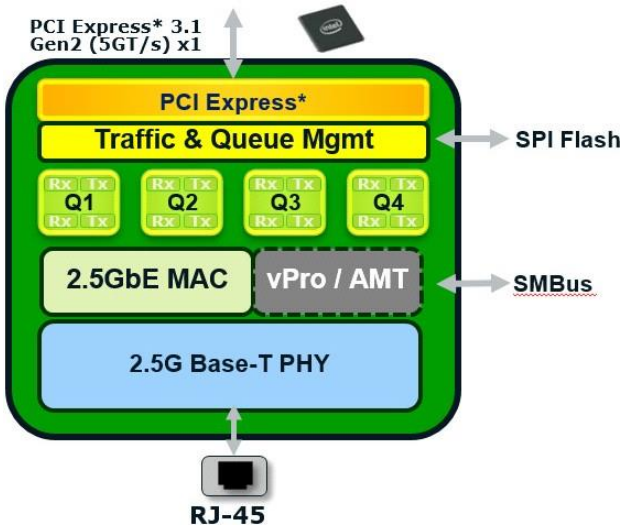

Figure 1-1. I225/I226 High level Functional View

1.1.1 Ethernet Interface

The I225/I226 implements an IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO interface), to the internal PHY. This interface provides the MAC and software the ability to monitor and control the state of the PHY. The MDIO interface defines a special protocol that runs across the connection, and an internal set of addressable registers. The interface consists of internal data line (MDIO) and clock line (MDC), which are accessible by software via the MAC register space.

1.1.2 Intel vPro® Interfaces

When the system is at its active state, the I225/I226 communicates with the Intel vPro® engine over PCIe. When the system is at low power state (Sx), the I225/I226 communicates with the Intel vPro® engine over SMBus. The I225/I226 and the Intel vPro® engine switch between these two interfaces according to the system power states (identified by the PCIe bus state).

The I225/I226 supports the SMBus at 1 MHz. This interface includes these open-drain signals:

- Data In/Out signal - SMB_DATA
- Clock signal - SMB_CLK

Default SMBUS Slave Address:

- 0x59 (address 0xB2) for LOM/Discrete/NIC design.
- 0x49 (address 0x92) for Docking Station design.

1.1.3 Configurable Software-Definable Pins (SDPs)

The I225/I226 also provides Software Defined Pins (SDPs) that can be used to drive or sense signals between external devices and the I225/I226. The SDP pin can be driven or sensed by the I225/I226 software or can be activated by the embedded 1588 timers.

1.1.4 Feature Summary

Table 1-1 through Table 1-6 lists the feature set provided by the I225/I226.

Table 1-1. General Features

Feature	I225/I226
Serial Flash interface	Y
Configurable LED operation for software or OEM custom-tailoring of LED displays	Y
Protected Flash space for private configuration	Y
Package size (mm x mm)	7x7
Extended temperature (special SKU)	I225IT
Industrial temperature (special SKU)	I226IT

Table 1-2. Network Features

Feature	I225/I226
2.5 Gbps BASE-T	Y
10BASE-Te, 100BASE-TX, 1000BASE-T	Y
Integrated BASE-T PHY	Y
MDI lane swap	Y
Half duplex at 10/100 Mb/s operation and full duplex operation at all supported speeds	Y
Jumbo frames support (with no TSN)	Y
Size of jumbo frames support	9.5 KB
Flow control support: send/receive PAUSE frames and receive FIFO thresholds	Y
802.1q VLAN support	Y
802.3az EEE support	Y

Table 1-3. Host Interface Features

Feature	I225/I226
PCIe* revision	3.1
PCIe* physical layer	Gen 2 (5.0GT/s)
PCIe* Bus width	x1
64-bit address support for systems using more than 4 GB of physical memory	Y
CSR access via configuration space	Y
TSN preemption, time aware shaper and interspersing	Y

Table 1-4. LAN Function Features

Feature	I225/I226
Programmable host memory receive buffers	Y
Descriptor ring management hardware for transmit and receive	Y
ACPI register set and power down functionality supporting D0 and D3 states	Y
Wake up	Y
Flexible wake-up filters	32
Flexible filters for queue assignment in normal operation	8
IPv6 wake-up filters	Y
Default configuration by the NVM Flash for all LEDs for pre-driver functionality	3 LEDs
Programmable memory transmit buffers	Y
Double VLAN	Y
IEEE 1588	Y
Per-packet time stamp	Y
Tx rate limiting per queue	Y

Table 1-5. LAN Performance Features

Feature	I225/I226
TCP segmentation offload Up to 256 KB	Y
IPv6 support for IP/TCP and IP/UDP receive checksum offload	Y
Fragmented UDP checksum offload for packet reassembly	Y
Message Signaled Interrupts (MSI)	Y
Message Signaled Interrupts (MSI-X) number of vectors	5
Interrupt throttling control to limit maximum interrupt rate and improve CPU utilization	Y
Rx packet split header	Y
Total number of Rx queues	4
Total number of TX queues	4
TSO interleaving for reduced latency	Y
SCTP receive and transmit checksum offload	Y

Table 1-6. Power Management Features

Feature	I225/ I226
ACPI register set and power down functionality supporting D0 and D3 states	Y
Full wake-up support (APM and ACPI 2.0)	Y
Smart power down at S0 no link and Sx no link	Y
PCIe function disable	Y
Dynamic device off	Y
Energy Efficient Ethernet (EEE)	I226 only
DMA coalescing	Y
Integrated SVR / LVR control	Y

1.2 Intel ® Ethernet Controller I226 - Highlights

Compared to I225, the I226 highlights state below:

- Dramatically reduced power consumption in all silicon states (20-50% reduction)
- Improved cable BER performance, especially on longer cables
- Ability to support industrial temperature fully (85°C) at 2.5G speeds
- Resolution for minor bug fixes, enhancements.
    - Please review *Intel® Ethernet Controller I225 Specification Update (Content ID 615084)*.

2.0 Pin Interface

The I225/I226 is a 56-pin, 7 x 7 mm VQFN package. A top level view of the pin layout is shown in Figure 2-1. The I/O pins are listed in Table 2-1.

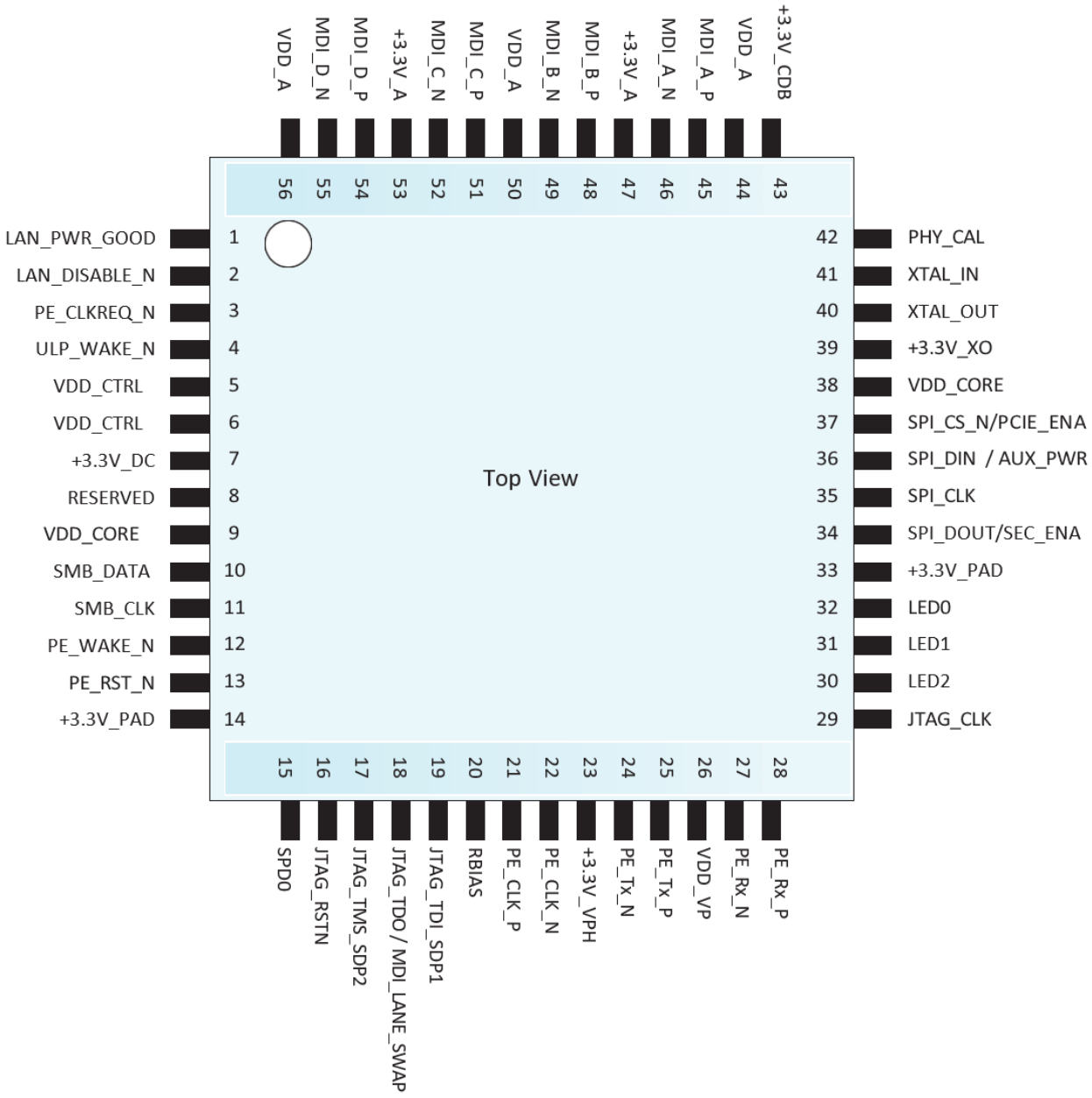

Figure 2-1. I225/I226 Pin Diagram (Top View)

Table 2-1. I225/I226 Pin List

Pin #	Pin Name	Internal Weak Pull Up/Down on Reset	Internal Weak Pull Up/Down During Normal Operation		Pin #	Pin Name	Internal Weak Pull Up/Down on Reset	Internal Weak Pull Up/Down During Normal Operation
1	LAN_PWR_GOOD	PU	PU		29	JTAG_CLK	PU	PU
2	LAN_DISABLE_N	PU	PU		30	LED2	PU	
3	PE_CLKREQ_N	PU			31	LED1	PU	
4	ULP_WAKE_N	PU			32	LED0	PU	
5	VDD_CTRL				33	+3.3V_PAD		
6	VDD_CTRL				34[1]	SPI_DOUT/ SEC_ENA	PU	PU
7	+3.3V_DC				35[1]	SPI_CLK	PU	PU
8	RESEVRED				36[1]	SPI_DIN/AUX_PWR	PU	PU
9	VDD_CORE				37[1]	SPI_CS_N/ PCIE_ENA	PU	PU
10	SMB_DATA	PU			38	VDD_CORE		
11	SMB_CLK	PU			39	+3.3V_XO		
12	PE_WAKE_N	PU			40	XTAL_OUT		
13	PE_RST_N	PU	PU		41	XTAL_IN		
14	+3.3V_PAD				42	PHY_CAL		
15	SDP0	PU	PU		43	+3.3V_CDB		
16	JTAG_RSTN	PD	PD		44	VDD_A		
17	JTAG_TMS_SDP2	PU	PU		45	MDI_A_P		
18	JTAG_TDO/ MDI_LANE_SWAP	PU	PU		46	MDI_A_N		
19	JTAG_TDI_SDP1	PU	PU		47	+3.3V_A		
20	RBIAS				48	MDI_B_P		
21	PE_CLK_P				49	MDI_B_N		
22	PE_CLK_N				50	VDD_A		
23	+3.3V_VPH				51	MDI_C_P		
24	PE_Tx_N				52	MDI_C_N		
25	PE_Tx_P				53	+3.3V_A		
26	VDD_VP				54	MDI_D_P		
27	PE_Rx_N				55	MDI_D_N		
28	PE_Rx_P				56	VDD_A		

1. The internal pull-ups are weak. They should not be used for the normal operation. It is recommended that these pins have external pull-ups as needed.

2.1 Signal Type Definition (Abbreviations)

Table 2-2. I/O Pin Type Abbreviations

Abbreviations	Description
I	Input-only, digital levels.
O	Output-only, digital levels.
I/O	Bidirectional In/Out digital levels signal.
Prg	Programmable Bidirectional digital levels.
PWR	Power.
AI	Input-only, analog levels.
AO	Output-only, analog levels.
AI/O	Bidirectional, analog levels.
GND	Ground.

2.2 Ethernet Media Interface

Table 2-3. Ethernet Media Interface

Pin #	Pin Name	Pin Type	MDI_LANE_ SWAP = 1 Functionality	MDI_LANE_ SWAP = 0 Functionality	Function
45	MDI_A_P	AI / AO	MDI_A_P	MDI_D_N	Media Dependent Interface. Connect four MDI pairs directly to the magnetics/RJ45 component. No external terminations are needed.
46	MDI_A_N	AI / AO	MDI_A_N	MDI_D_P	
48	MDI_B_P	AI / AO	MDI_B_P	MDI_C_N	
49	MDI_B_N	AI / AO	MDI_B_N	MDI_C_P	
51	MDI_C_P	AI / AO	MDI_C_P	MDI_B_N	
52	MDI_C_N	AI / AO	MDI_C_N	MDI_B_P	
54	MDI_D_P	AI / AO	MDI_D_P	MDI_A_N	
55	MDI_D_N	AI / AO	MDI_D_N	MDI_A_P	
42	PHY_CAL	Calibration for all GPHY Ethernet ports.			

2.3 PCIe Interface

Table 2-4. PCIe Interface

Pin #	Pin Name	Pin Type	Function
28	PE_Rx_P	AI	Differential PCIe Receive Pair. These pins must be AC-coupled.
27	PE_Rx_N	AI	
25	PE_Tx_P	AO	Differential PCIe Transmit Pair. These pins must be AC-coupled.
24	PE_Tx_N	AO	
20	RBIAS	AI/O	Pad to connect external tuning resistor.
21	PE_CLK_P	AI	Differential PCIe Clock Pair. The input clock is 100 MHz external reference clock used by the PHY.
22	PE_CLK_N	AI	
13	PE_RST_N	I	PCIe Reset. Power and Clock Good Indication. The PE_RST_N signal indicates that both PCIe power and clock are available.
12	PE_WAKE_N	I/O	PCIe Wake. This signal is driven to zero (0V) when it detects a wake-up event and either:
3	PE_CLKREQ_N	I/O	PCIe Clock Request. This PCIe CLKREQ# is for power management.

2.4 Management and SPI Flash Interfaces

Table 2-5. Management Interfaces

Pin #	Pin Name	Pin Type	Function
SMBus Interface			
4	ULP_WAKE_N	I/O	ULP Wake. This pin is used by the external Management Controller (CSME) to wake the device from ULP.
11	SMB_CLK	I/O	SMBus Clock. Must connect to PCH's SML0_CLK pin. One clock pulse is generated for each data bit transferred. Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499 Ω resistor to support 1 MHz (while in Sx mode). The resistor value might be adjusted to a higher value to meet the VOH and VOL voltage-level requirements. Refer to the I225/I226 Design Checklist for more detail.
10	SMB_DATA	I/O	SMBus Data. Connect to PCH's SML0_DAT channel. Stable during the high period of the clock (unless it is a start or stop condition). Pull this signal up to 3.3 Vdc (auxiliary supply) through a 499 Ω resistor to support 1 MHz (while in Sx mode). The resistor value might be adjusted to a higher value to meet the VOH and VOL voltage-level requirements. Refer to the I225/I226 Design Checklist for more detail.
SPI Master Interface			
34	SPI_DOUT/ SEC_ENA	O	SPI Data Output. This pin is also SPI Flash Security strapping. During normal operation, this pin should be connected to an external 10 KΩ pull-up resistor. Holding Low on this pin will not disable Firmware Authentication (Contend ID #632906).
36	SPI_DIN/AUX_PWR	I	SPI Data Input. This pin is also the AUX_PWR strapping. An external 10 KΩ pull-up resistor is required in systems on which the device gets power during D3cold. In Network Interface Card (NIC) designs this pin should be connected as shown in Figure 2- 2.
35	SPI_CLK	O	SPI Clock. During normal operation, this pin should be connected to an external 10 KΩ pull- down resistor.
37	SPI_CS_N/ PCIE_ENA	O	SPI Chip Select. Active low signal. During normal operation, this pin should be connected to an external 10 KΩ pull-up resistor.

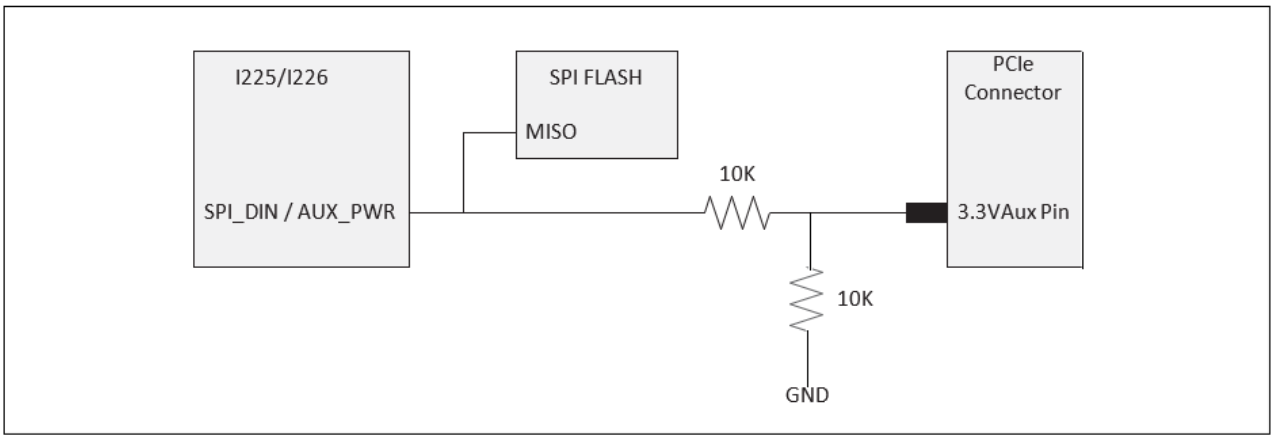

Figure 2-2. AUX_PWR Strapping Connection

2.5 LED / JTAG / UART Interface

Table 2-6. LED/UART/JTAG Interface

Pin #	Pin Name	Pin Type	Function
32	LED0	0	LED0. This signal is used for the programmable LED.
31	LED1	0	LED1. This signal is used for the programmable LED.
30	LED2	0	LED2. This signal is used for the programmable LED.
29	JTAG_CLK	I	JTAG Test Clock. The signals TDI, TDO and TMS are synchronous subject to this JTAG test clock.
16	JTAG_RSTN	I	JTAG Test Reset. At low, the JTAG is in the reset state and the multiplexed pins JTAG/SDPs act as SDPs. This pin has an internal weak pull-down that holds the JTAG controller in its reset state if the pin is left open.
17	JTAG_TMS_SDP2		JTAG Test Mode Select. Software
18	JTAG_TDO/ MDI_LANE_SWAP	O / Prg	JTAG Serial Test Data Output. MDI Lane Swap Configuration. This pin is also for the MDI lane swap strapping pin. It has an internal weak pull- up resistor and should be connected to an external 10 KΩ resistor if needed to be sampled at a low level. At a high level, all MDI lanes are default. MDI pins are shown in Figure 2-1. At a low level (when strapped), all MDI lanes are swapped. Refer to the *I225/I226 Lane Swap Configuration and Reference Schematic* for more detail.
19	JTAG_TDI_SDP1	I	JTAG Serial Test Data Input. Software

2.6 Miscellaneous Signals

Table 2-7. Miscellaneous Signals

Pin #	Pin Name	Pin Type	Function
41	XTAL_IN	AI	Crystal — Oscillator Input. A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must also tie both pins to ground.
40	XTAL_OUT	AO	Crystal — Oscillator Output. A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must also tie both pins to ground.
15	SDP0	Prg	Software Defined Pin 0 (SDP0). This pin can be selected as input or output mode.
1	LAN_PWR_GOOD	I	LAN Power Good. A 3.3 Vdc input signal. A transition from low-to-high initializes the I225/I226 into operation.
2	LAN_DISABLE_N	I	LAN Disable Input. This is a 3.3 Vdc input signal for D3Cold support only. ***Note:*** This pin is asynchronous.
5, 6	VDD_CTRL	AO	Internal SVR control pin (SVR switching Node). Connect to a 1.0 µH inductor and capacitors to provide a 0.95V rail with a worst-case tolerance ±10%.

2.7 Power Supply

Table 2-8. Power Supply

Pin #	Pin Name	Pin Type	Function
7	+3.3V_DC	PWR	DCDC Power Supply. This supply must provide a nominal voltage of 3.3 Vdc with a worst-case tolerance ±10%.
14, 33	+3.3V_PAD	PWR	Pad-Voltage Domain Supply. This supply must provide a nominal voltage of 3.3 Vdc with a worst-case tolerance ±10% at the corners, respectively. ***Note:*** Short cutting this voltage domain with others of same nominal value is not allowed on the I225/I226. For optimal power-consumption figure of merits, the lowest possible voltage must be selected in the system.
23	+3.3V_VPH	PWR	PCIe High-Voltage Domain Supply. This supply must provide a nominal voltage of 3.3 Vdc with a worst-case tolerance ±10%.
39	+3.3V_XO	PWR	XO Pad-Voltage Domain P Supply. This supply must provide a nominal voltage of 3.3 Vdc with a worst-case tolerance ±10%.
43	+3.3V_CDB	PWR	CDB High-Voltage Domain Supply. This supply must provide a nominal voltage of 3.3 Vdc ±10%.
47, 53	+3V3_A	PWR	High-Voltage Domain Supply. This is the group of supply pins for the high voltage domain. It supplies the AFE of the GbE PHY. This supply must provide a nominal voltage of 3.3 Vdc with a worst-case tolerance ±10% at the corners, respectively.
26	VDD_VP	PWR	PCIe Low-Voltage Domain Supply. This supply must provide a nominal voltage of 0.95 Vdc with a worst-case tolerance ±10%.

Table 2-8. Power Supply

Pin #	Pin Name	Pin Type	Function
9, 38	VDD_CORE	PWR	Core-Voltage Domain Supply. This supply must provide a nominal voltage of 0.95 Vdc with a worst-case tolerance ±10%.
44, 50, 56	VDD_A	PWR	Low-Voltage Domain Supply. This is the group of supply pins for the low voltage domain. It supplies mixed signal blocks in the AFE and CDB of the GbE PHY. This supply must provide a nominal voltage of 0.95 Vdc with a worst-case tolerance ±10%.
8	Reserved	PWR	Fusing Domain Supply. During normal operation this pin should be tied to ground.
EPAD	EPAD	GND	General Device Ground. The EPAD* is the exposed pad at the bottom of the package. This pad must be properly connected to the ground plane of the Printed Circuit Board (PCB).

2.7.1 Leakage Avoidance on LAN Power Disconnect

When the I225/I226 is completely powered down using a FET to cut off the +3.3V_LAN power supply, there might be leakage on these five pins:

- Pin 3 — PE_CLKREQ_N
- Pin 4 — ULP_WAKE_N
- Pin 10 — SMB_DATA
- Pin 11 — SMB_CLK
- Pin 12 — PE_WAKE_N

To avoid leakage, a basic logic MOSFET can be setup to prevent the leakage path. Refer to the I225/I226 Design Checklist for more detail.

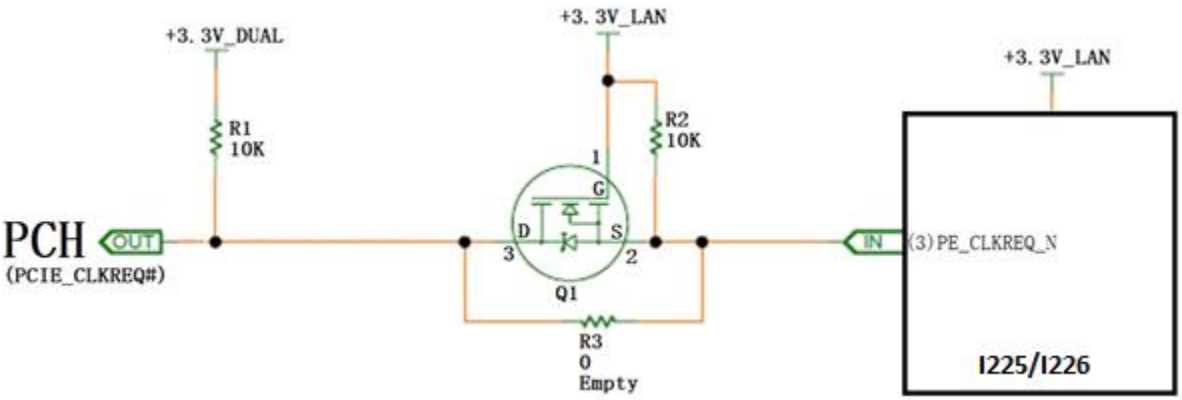

Figure 2-3. Leakage Protection Circuit

3.0 Interconnects

3.1 PCIe Interface

The I225/I226 is connected to the platform when the system is at its active state by a one lane PCIe gen 2 (5.0 GT/s) version 3.1 interface. This interface includes the following signals:

- Serial differential pair running at 5 Gb/s for Rx - RX0 pair.
- Serial differential pair running at 5 Gb/s for Tx - TX0 pair.
- 100 MHz differential clock input - PE_CLK pair.
- Power and clock good indication - PE_RSTn.
- Clock control signal - CLKREQn.
- System wakeup signal - PE_WAKEn

3.2 Non-Volatile Memory (NVM) Flash

3.2.1 General Overview

The I225/I226 uses a Flash device for storing product configuration information. The Flash is consist of several blocks listed in the sections that follow, summarized in Table 3-1 and shown in Figure 3-1. More granular modules in the NVM are listed in Table 3-1. The various blocks and its programming method are detailed in the following sections. For its operation the I225/I226 requires a 1 MB Flash as a minimum and a 2 MB Flash if OROM is needed.

- **Legacy EEPROM** - Hardware accessed modules (**Block 0** and **Block 1**) — Loaded by the I225/I226 hardware after power-up, PCI reset de-assertion, D3 to D0 transition, or software reset. Different hardware sections in the Flash are loaded at different events. The hardware block is loaded to a shadow RAM in the device. It is located at the first 2 x 4 KB sectors in the Flash.
- **Secured Image** (**Block 2**) — The following data sections are protected by an RSA signature:
  - **CSS Header** - The CSS header describes the modules within the protected block and includes the security signature of the block. The CSS header is counted as part of the firmware module for the sake of its size in the NVM.
  - **Firmware Module** - The firmware module contains the code for the embedded controller, a list of supported Flash devices and a RO update section. The firmware module is loaded at power up and firmware reset.
  - **PHY Module** - The PHY code is loaded by the PHY cluster for its functionality following a power up or any reset that affect the PHY.
  - **Expansion/Option ROM Module** (OROM Module) - This block is optional and might exist only on larger Flash sizes than 1 MB. It holds code that is expected to be executed by the system at pre-operating system state. The option ROM module might include the following sub-modules: PXE driver, iSCSI boot image, UEFI network driver and can also include a CLP module.
- **Free Provisioning Module** (**Block 3**) — This block is used by software to program a new secured image.

- **mDNS Records A / B (Block3 / Block 4)** — The mDNS records are used by the CSME firmware for mDNS offload proxy while the system is in D3. It is software's responsibility to program these records before entering the D3 state. The mDNS records are expected to reside adjacent to the firmware space. So, the mDNS records are stored in the A space or B space (as shown in Figure3- 1) depending in the location of the secured image.
- **Software Free Access Module (Block 4)** — This module is used mainly by software. It also contains the mDNS records used by the Manageability Engine (ME) firmware for mDNS offload proxy while the system is in D3. Note that the structure of this block is outside the scope ofthis document.

Table 3-1. NVM Modules

Module Name	Module Size	Module Pointer Location
Shadow RAM Sector 0	4 KB	Module starts at absolute address 0 in the Flash.
Shadow RAM Sector 1	4 KB	Module starts at absolute address 4 KB in the Flash.
CSS Header	inc. in FW Module	Word offset 0x10 in the shadow RAM.
Firmware Module	364 KB	The address is defined in the CSS header.
PHY Module	128 KB	Word offset 0x7F0 in the shadow RAM.
OROM Module	512 KB	Offset 0x4A in the shadow RAM.
Free Provisioning Space	1004 KB	Offset 0x40 in the shadow RAM.
Software Free	16 KB	Word offset 0x7F1 in the shadow RAM.
mDNS Records	16 KB	Offset 0x25 in the shadow RAM.
All previous pointers are 16-bit words. The most significant bit of these pointers is set to 1b stating that the pointers define an absolute address outside the shadow RAM space. The other 15 least significant bits of these pointers specify an address defined in 4 KB units.		

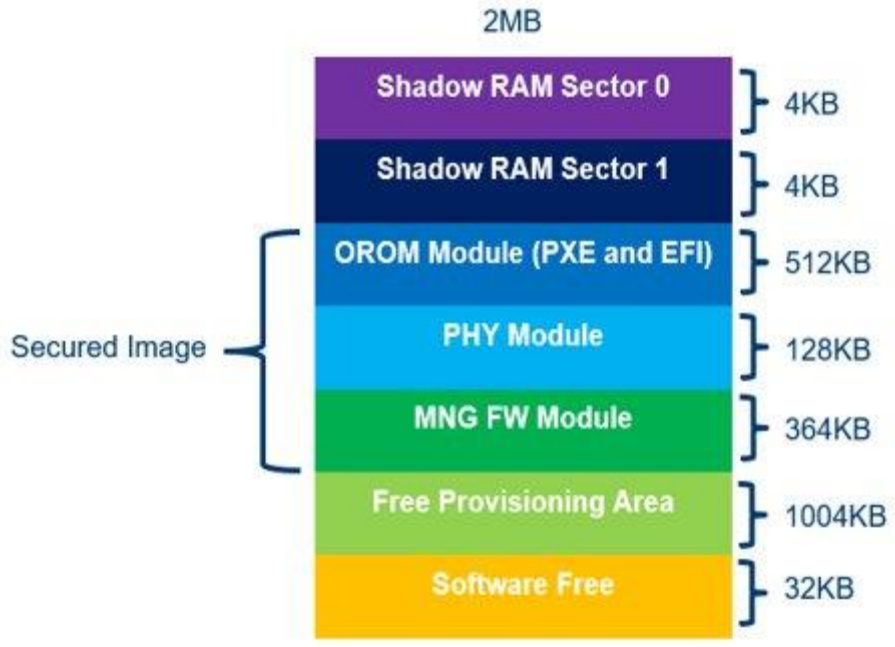

Figure 3-1. NVM Structure

Note: This document uses the terms NVM and Flash to refer to the non-volatile memory used by the I225/I226. both terms have the same meaning.

3.2.2 NVM Security

The NVM update is protected by secured integrity check. It ensures that only an Intel approved image can be updated on I225/I226 devices after manufacturing. The updated image is checked against a digital SHA256 signature that is then encrypted by a private 2048-bit RSA Intel key. The modules that are protected by the secured integrity check are:

- Optional OROM module
- PHY module
- Firmware module

Any updated image includes all these secured modules.

3.2.3 Shadow RAM

The I225/I226 maintains the first two 4 KB sectors, Sector 0 and Sector 1 (block 0 and block 1), for the hardware configuration content. At least one of these two sectors must be valid at any given time or else the I225/I226 is set by hardware default. Following a Power On Reset (POR), the I225/I226 copies the valid lower 4 KB sector of the Flash device into an internal shadow RAM. Any further accesses of the software or firmware to this section of the NVM are directed to the internal shadow RAM. After a software command, modifications made to the shadow RAM content are then copied by the I225/I226 manageability into the other 4 KB sector of the NVM, flipping circularly the valid sector between sector 0 and 1 of NVM.

This mechanism provides the following advantages:

1. A seamless backward compatible read/write interface for software/firmware to the first 4 KB of the NVM as if an external EEPROM device was connected. This interface is referred as EEPROM-mode access to the Flash.
2. A way for software to protect image-update procedure from power down events by establishing a double-image policy. It relies on having pointers to all the other NVM modules mapped in theNVM sector that is mirrored in the internal shadow RAM.
3. A way to ensure that a hardware auto-load event, which occurs further to a PCIe reset event, can be completed within the PCIe timing constraints (100 ms) even if the Flash is occupied performing an erase operation initiated just before the reset.

Due to NVM security reasons, hardware does not allow any Flash accesses until the NVM is authenticated and the Flash blocks are identified by the device.

3.2.4 Protected Areas and Words

The I225/I226 provides a mechanism to protect against programming (write access) specific areas in the Flash as follows:

- The two shadow RAM sectors (the first 8 KB of the Flash device) are write protected. During normal operation, this area is programmed only by the device (autonomously) following a request from the software updating the shadow RAM.
- The secured block containing the CSS header, firmware content, PHY cluster content and the OROM module is also write protected. Updating the secured block, software can program the free provisioning area and request the device to make it the next valid secured block. Once it is authenticated by the device, it becomes the valid secured block and then it is write protected.

The following table lists the protected words in the shadow RAM space.

Table 3-3. Protected Words List

Word Offset	Word Name	Word Offset	Word Name
0x00..0x02	Ethernet Individual MAC Address	0x2D	Start of RO Area
0x03	Compatibility Bytes	0x2F	VPD Pointer
0x08	PBA Number 0	0x34	PCIe PHY Configuration 0 Low
0x09	PBA Number 1	0x35	PCIe PHY Configuration 0 High
0x0D	Device ID	0x37	Alternate MAC Address Location
0x0E	Vendor ID	0x38	PCIe PHY Configuration 1 Low
0x0A	VPD Enable Flag	0x39	PCIe PHY Configuration 1 High
0x10	Secure Area Start Address	0x3A	PCIe PHY Configuration 2 low/Reset to PCIe PHY Delay (0x40 µs)
0x11	Flash Device Size	0x3C	PXE VLAN Pointer
0x12	EEPROM Sizing and Protected Fields	0x3D	iSCSI Boot Configuration Pointer
0x17	Software Reset CSR Auto Configuration Pointer	0x40	Free Provisioning Area Pointer
0x22	LAN Power Consumption	0x41	Free Provisioning Area Size
0x23	PCIe Reset CSR Auto Configuration Pointer	0x44	PCIe L1 Sub-states Capability Low
0x24	Initialization Control 3	0x45	PCIe L1 Sub-states Capability High
0x25	mDNS Records Area Offset	0x46	PCIe L1 Sub-states Control First Low
0x26	mDNS Records Area Size	0x47	PCIe L2 Sub-states Control First High
0x27	CSR Auto Configuration Power-up Pointer	0x48	PCIe L2 Sub-states Control Second
0x28	PCIe Control 2	0x4A	EXP.ROM Boot Code Section Pointer
0x2A	CDQM Memory Base Low	0x50	RO Commands Version
0x2B	CDQM Memory Base High	0x51	Firmware Module Configuration Pointer
0x2C	End of Read-only (RO) Area		

3.3 Network Interfaces

3.3.1 Overview

The I225/I226 provide a complete CSMA/CD function with an integrated MAC and PHY. It supports the following link speeds: 10 Mb/s; 100 Mb/s; 1000 Mb/s and 2.5 Gb/s. Full Duplex is supported at all link speed while Half Duplex is supported at 10 Mb/s; 100 Mb/s only.

3.4 Configurable LED Outputs

The I225/I226 provides three LEDs / GPIO pins that can be used to indicate different speed status of the link. The default setup of the LEDs is loaded from the NVM word offsets 0x1C and 0x1F. This setup is reflected in the LEDCTL register. The software device driver can change this setup accessing the LEDCTL register. For each of the LEDs, the following parameters can be defined:

- LED Functionality (Mode): Defines which information is reflected by this LED as listed in Table3-4.
- Polarity (IVRT): Defines the polarity of the LED.
- Blink mode (BLINK): Determines whether or not the LED should blink or be stable. In addition, the blink rate of all LEDs can be defined by the *Global Blink Mode* flag in the LEDCTL register. The possible rates are 200 ms or 83 ms for each phase. There is one rate for all theLEDs.

Table 3-4. Link Mode Encoding

LEDx_MODE (x=0...3)	LED Functionality
0x0	LED_ON - Always high (Asserted)
0x1	LED_OFF - Always low (De-asserted)
0x2	LINK_UP - Asserted when any speed link is established
0x3	FILTER_ACTIVITY - Asserted when link is established and packets are being transmitted or received that passed MAC filtering
0x4	LINK_ACTIVITY - Asserted when link is established and when there is no transmit or receive activity. When BLINK is set, the LED is on if there is link and it blinks for activity (either receive or transmit).
0x5	LINK_10 - Asserted when a 10 Mb/s link is established
0x6	LINK_100 - Asserted when a 100 Mb/s link is established
0x7	LINK_1000 - Asserted when a 1000 Mb/s link is established
0x8	LINK_2500 - Asserted when a 2500 Mb/s link is established
0x9	SDP_MODE - The SDP pin functions as an SDP. SDP0...2 on LED 0...2 pins respectively.
0xA	PAUSED - Asserted when the transmitter is PAUSED by the flow scheme
0xB	ACTIVITY - Asserted when link is established and packets are being transmitted or received
0xC	LINK_10/100 - Asserted when either 10 or 100 Mb/s link is established
0xD	LINK_100/1000 - Asserted when either 100 or 1000 Mb/s link is established and maintained
0xE	LINK_1000/2500 - Asserted when either 1000 or 2500 Mb/s link is established
0xF	LINK_100/2500 - Asserted when either 100 or 2500 Mb/s link is established and maintained
The dynamic LED modes (FILTER_ACTIVITY, LINK/ACTIVITY, ACTIVITY, PAUSED) should be used with LED Blink mode enabled.	

3.5 Transmission of PAUSE Frames

The I225/I226 generates PAUSE packets to ensure there is enough space in its receive packet buffers to avoid packet drop. The I225/I226 monitors the fullness of its receive packet buffers and compares it with the contents of a programmable threshold. When the threshold is reached, the I225/I226 sends a PAUSE frame. The I225/I226 supports the sending of link Flow Control (FC).

3.5.1 Operation and Rules

Transmission of link PAUSE frames is enabled by software writing a 1b to the *TFCE* bit in the Device Control register.

The I225/I226 sends a PAUSE frame when Rx packet buffer is full above the high threshold defined in the Flow Control Receive Threshold High (*FCRTH0.RTH*) register field. When the threshold is reached, the I225/I226 sends a PAUSE frame with its pause time field equal to *FCTTV*. The threshold should be large enough to overcome the worst case latency from the time that crossing the threshold is sensed until packets are not received from the link partner. The Flow Control Receive Threshold High value should be calculated as follows:

Flow Control Receive Threshold High = Internal Rx Buffer Size - (Threshold Cross to XOFF Transmission + Round-trip Latency + XOFF Reception to Link Partner response)

Parameter values to be used for calculating the *FCRTH0.RTH* value are listed in Table 3-5.

3.5.2 Software Initiated PAUSE Frame Transmission

The I225/I226 has the added capability to transmit an XOFF frame via software. This is accomplished by software writing a 1b to the *SWXOFF* bit of the Transmit Control register. Once this bit is set, hardware initiates the transmission of a PAUSE frame in a manner similar to that automatically generated by hardware.

The *SWXOFF* bit is self-clearing after the PAUSE frame has been transmitted.

Note: The Flow Control Refresh Threshold mechanism does not work in the case of software- initiated flow control. Therefore, it is the software's responsibility to re-generate PAUSE frames before expiration of the pause counter at the other partner's end.

3.6 Energy Efficient Ethernet (EEE)

Energy Efficient Ethernet (EEE) Low Power Idle (LPI) mode defined in IEEE802.3az optionally enables power saving by switching off part of the LAN device functionality when no data needs to be transmitted or/ and received. The decision as to whether or not the LAN device transmit path should enter LPI mode or exit LPI mode is done according to transmit needs. Information as to whether or not a link partner has entered LPI mode is detected by the LAN device and is used for power saving in the receive circuitry.

I225 doesn't support EEE, but I226 does support EEE

When no data needs to be transmitted, a request to enter transmit LPI is issued on the internal xxMII Tx interface causing the PHY to transmit sleep symbols for a pre-defined period of time followed by a quiet period. During LPI, the PHY periodically transmits refresh symbols that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. This quiet- refresh cycle continues until transmitting normal inter-frame encoding on the internal xxMII interface. The PHY communicates to the link partner the move to active link state by sending wake symbols for a pre-defined period of time. The PHY then enters a normal operating state where data or idle symbols are transmitted.

In the receive direction, entering LPI mode is triggered by receiving sleep symbols from the link partner. This signals that the link partner is about to enter LPI mode. After sending the sleep symbols, the link partner ceases transmission. When a link partner enters LPI, the PHY indicates assert low power idle on the internal xxMII RX interface and the LAN device's receiver disables certain functionality to reduce power consumption.

Figure 3-2 shows, and Table 3-6 lists the general principles of EEE LPI operation on the Ethernet Link.

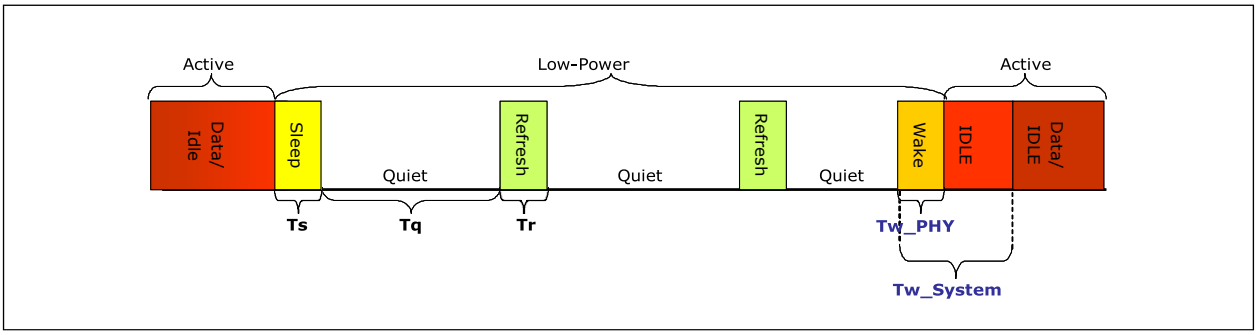

Figure 3-2. Energy Efficient Ethernet Operation

Table 3-6. Energy Efficient Ethernet Parameters

Parameter	Description
Sleep Time (Ts)	Duration PHY sends sleep symbols before going quiet.
Quiet Duration (Tq)	Duration PHY remains quiet before it must wake for refresh period.
Refresh Duration (Tr)	Duration PHY sends refresh symbols for timing recovery and coefficient synchronization.
PHY Wake Time (Tw_PHY)	Minimum duration PHY takes to resume to an active state after decision to wake.
Receive System Wake Time (Tw_System_rx)	Wait period where no data is expected to be received to give the local receiving system time to wake up.
Transmit System Wake Time (Tw_System_tx)	Wait period where no data is transmitted to give the remote receiving system time to wake up.

3.6.1 EEE Auto-Negotiation

Auto-negotiation provides the capability to negotiate EEE capabilities with the link partner using the next page mechanism defined in IEEE802.3 Annex 28C. IEEE802.3 auto-negotiation is performed at power up, on command from software, upon detection of a PHY error or following linkre-connection.

During the link establishment process, both link partners indicate their EEE capabilities via the IEEE802.3 auto-negotiation process. If EEE is supported by both link partners for the negotiated PHY type, then the EEE function can be used independently in either direction.

The I226 supports EEE auto-negotiation. EEE capabilities advertised during auto-negotiation can be modified via the *EEEEEE_2_5G_AN*, *EEE_1G_AN* and *EEE_100M_AN* flags in the IPCNFG register.

4.0 Power Management and Power Consumption

4.1 Power Management

The I225/I226 supports an intelligent power management scheme. The three global power states are as follows:

- When the system is at its functional state it auto-negotiates the link speed to the highestcommon denominator for best performance.
- When the system is at its low power state, the I225/I226 can be configured to auto-negotiate the link to lower speeds, saving system power.
- The I226 can be put into an Ultra-Low Power (ULP) state when the link is disconnected.
  - Platform hardware needs to connect I226's LAN_DISABLE_N pin to a GPIO at either platform or EC.
  - System BIOS will need to implement the _On/ _Off method on the GPIO pin.
    - **Enable ULP entry on D3Cold entry:** the _On method should de-assert (drive HIGH) GPIO connected to LAN_DISABLE_N.
    - **Exit ULP on D3Cold exit:** _Off method should assert (drive LOW) LAN_DISABLE_N.
  - There are three ways to exit ULP:
    - ULP by the user — Cable detected event (user plugs in the LAN cable).
    - ULP by the host — On exit from RTD3, the operating system calls the BIOS _ON method that can be assigned to de-assert the LAN_DISBALE_N pin using GPIO. This event causes ULP to exit.
    - ULP by CSME — The CSME can trigger a ULP exit by asserting the ULP_WAKE_N pin. This can be done by connecting SMB_DATA to ULP_WAKE_N.

4.2 General Power State Information

4.2.1 PCIe Device Power States

- D0 — Device is fully on. The I225/I226 is completely active (L0), in the link idle condition (L0s)or transitions to a link lower power state (L1).
- D1 and D2 — Not supported.
- D3hot — Where primary power is maintained. D3hot enters L1 to support clock removal on mobile platforms (for power saving feature).
- D3cold — Where primary power can be removed. If auxiliary power is still available, the I225/I226 can support wake-capable logic (L3).

4.2.2 PCIe Link Power States

- L0 — Link up (active). L0s is the link in the idle condition.
- L1 — PCIe link low power states, L1.1 or L1.2
- L2 — Support device D3cold with auxiliary power is still maintained. Note that sideband PE_WAKE_N signaling exists to cause wake-capable devices to exit this state. The power saving opportunities for this state include, but are not limited to, shutdown of all transceiver circuitry except detection circuitry to support exit, clock gating of all PCIe logic and shutdown of the PLLas well as appropriate platform voltage and clock generators.
- L3 — Link completely down (off). Power and clock are removed in this link state and there is no auxiliary power available. To bring the I225/I226 and its link back up, the platform must go througha boot sequence where power, clock and reset are reapplied appropriately.

4.3 I225 Power Consumption

Note: All data measured using I225 Reference Add-on Cards

System State	Device State	Ethernet Link State	Power (mW) @ 3.3V	
			iSVR, 3-meter Cable, 25 °C	iSVR, 100-meter Cable, 55 °C
S0	D0	2.5G Max TDP	-	2,200
		2.5G Active	1,214	1,882
		2.5G Idle	885	1,572
		1G Active	715	788
		1G Idle	654	707
		100M Active	415	446
		100M Idle	378	403
		10M Active	416	443
		10M Base-Te Idle	345	363
		Cable Disconnected	250	250
S0ix/Sx WOL Enabled	D3Cold	2.5G	885	1,572
		1G	654	707
		100M	378	403
		10M Base-Te	345	363
		Cable Disconnected	250	250

4.4 I226 Power Consumption

Note: All data measured using I226 Reference Add-On Cards

System State	Device State	Ethernet Link State	Power (mW) @ 3.3V	
			iSVR, 3-meter Cable, 25 °C	iSVR, 100-meter Cable, 55 °C
S0	D0	2.5G Max TDP	-	1,480 (IT SKU) 1,300 (LM/ V)
		2.5G Active	910	1,185
		2.5G Idle	762	1,005
		2.5G Idle (EEE)	600	717
		1G Active	695	825
		1G Idle	562	665
		1G Idle (EEE)	290	355
		100M Active	405	470
		100M Idle	292	345
		100M Idle (EEE)	220	270
		10M Active	400	462
		10M Base-Te Idle	255	305
		Cable Disconnected (Ultra-Low Power)	17	17
S0ix/Sx WOL Enabled	D3Cold	2.5G (EEE)	587	710
		1G (EEE)	289	340
		100M (EEE)	220	270
		10M Base-Te	255	305
		Cable Disconnected (Ultra-Low Power)	17	17

5.0 Non-Volatile Memory Map

5.1 NVM General Summary Table

Word Address	Used By	Word Name	Reference
0x0000	HW	Ethernet Individual Address 0	36
0x0001	HW	Ethernet Individual Address 1	36
0x0002	HW	Ethernet Individual Address 2	36
0x0003	SW	Compatibility Bytes	37
0x0004-10	SW	Reserved (OEM Configuration)	-
0x000A	HW	Initialization Control Word 1	37
0x000B	HW	Subsystem ID	38
0x000C	HW	Subsystem Vendor ID	38
0x000D	HW	Device ID	38
0x000E	HW	Vendor ID	38
0x000F	HW	Initialization Control Word 2	38
0x0012	HW	EEPROM Sizing and Protected Fields	40
0x001C	HW	LED 1 Configuration Defaults	40
0x001F	HW	LED 0,2 Configuration Defaults	41
0x0022	HW	LAN Power Consumption	41
0x0030	HW	Setup Options PCI Function	41
0x0032	HW	PXE Version	43
0x0033	HW	IBA Capabilities	43
0x003F	SW	Checksum Word	44
0x0044	SW	PCIe L1 Substates Capability Low	45
0x0045	SW	PCIe L1 Substates Capability High	45
0x0046	SW	PCIe L1 Substates Capability 1st Low	45
0x004B	SW	ULP Capability Enable	45
0x004C - 0x007F	HW	Reserved	-

5.1.1 Common and Lan Port 0 Section Summary Table

Start of Shadow RAM - Sector 0.

5.1.1.1 Ethernet Individual Address 0 - 0x0000

The Ethernet Individual Address (IA) is a 6-byte field that must be unique for each NIC, and thus unique for each copy of the EEPROM image. The first three bytes are vendor specific. For example, the IA is equal to [00 AA 00] or [00 A0 C9] for Intel products. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0).

The Ethernet address is loaded for LAN0 from Addresses 0x0 to 0x02 and for LAN 1, 2 and 3 from offsets 0x0 to 0x2 at the start of the relevant sections.

Bits	Field Name	Description
15:0	Ethernet Individual Address 0	

5.1.1.2 Ethernet Individual Address 1 - 0x0001

The Ethernet Individual Address (IA) is a 6-byte field that must be unique for each NIC, and thus unique for each copy of the EEPROM image. The first three bytes are vendor specific. For example, the IA is equal to [00 AA 00] or [00 A0 C9] for Intel products. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0).

The Ethernet address is loaded for LAN0 from Addresses 0x0 to 0x02 and for LAN 1, 2 and 3 from offsets 0x0 to 0x2 at the start of the relevant sections.

Bits	Field Name	Description
15:0	Ethernet Individual Address 1	

5.1.1.3 Ethernet Individual Address 2 - 0x0002

The Ethernet Individual Address (IA) is a 6-byte field that must be unique for each NIC, and thus unique for each copy of the EEPROM image. The first three bytes are vendor specific. For example, the IA is equal to [00 AA 00] or [00 A0 C9] for Intel products. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0).

The Ethernet address is loaded for LAN0 from Addresses 0x0 to 0x02 and for LAN 1, 2 and 3 from offsets 0x0 to 0x2 at the start of the relevant sections.

Bits	Field Name	Description
15:0	Ethernet Individual Address 2	

5.1.1.4 Compatibility Bytes - 0x0003

Bits	Field Name	Description
15:13	Reserved	Reserved
12	IT (Extended Temperature)	
11	NIC/LOM	NIC/LOM (0=NIC; 1=LOM)
10	Server card	Server card (0=Client; 1=Server)
9	Client card	Client card (0=Server; 1=Client)
8	Retail/OEM card	Retail/OEM card (0=Retail; 1=OEM)
7:6	Reserved	Reserved
5	Reserved	Reserved
4	Reserved	SMBus connected (0=Not Connected; 1=Connected)
3	Reserved	Reserved
2	PCI bridge NOT present	PCI bridge NOT present (0=PCI bridge NOT present; 1=PCI bridge present)
1:0	Reserved	Reserved

5.1.1.5 Initialization Control Word 1 - 0x000A

Bits	Field Name	Default NVM Value	Description
15	OTP_LOCK_EN	0x0	
14	Reserved	0x1	Reserved
13	LTR_EN	0x1	LTR capabilities reporting enable. 0 - Do not report LTR support in the PCIe configuration Device Capabilities 2 register. 1 - Report LTR support in the PCIe configuration Device Capabilities 2 register. Defines default setting of LTR capabilities reporting. Valid values are: 0x0 - Do not report LTR support in the PCIe configuration space. 0x1 - Report LTR support in the PCIe configuration Device Capabilities 2
12	VPD_EN	0x0	
11:7	reserved	0x0	
6	Reserved	0x0	Reserved.
5	Deadlock Timeout Enable	0x1	If set, a device granted access to the EEPROM or Flash that does not toggle the interface for more than 2 seconds will have the grant revoked.
4	LAN PLL Shutdown Enable	0x0	Reserved
3	Reserved	0x1	Reserved
2	DMA clock gating	0x1	When set Disables DMA clock gating power saving mode.
1	Load Subsystem IDs	0x1	When this bit is set to 1b the device loads its PCIe Subsystem ID and Subsystem Vendor ID from the EEPROM (Subsystem ID and Subsystem Vendor ID EEPROM words).
0	Reserved	0x1	Reserved

5.1.1.6 Subsystem ID - 0x000B

If the Load Subsystem IDs in Initialization Control Word 1 EEPROM word is set, the Subsystem ID word in the

Common section is read in to initialize the PCIe Subsystem ID. Default value is 0x0.

Bits	Field Name	Description
15:0	Subsystem ID	

5.1.1.7 Subsystem Vendor ID - 0x000C

If the Load Subsystem IDs bit in Initialization Control Word 1 EEPROM word is set, theSubsystem Vendor ID word in the Common section is read in to initialize the PCIe Subsystem Vendor ID. The default value is 0x8086.

Bits	Field Name	Description
15:0	Subsystem Vendor ID	Request of TME to set the value to 0xffff

5.1.1.8 Device ID - 0x000D

Bits	Field Name	Default NVM Value	Description
15:0	Device ID	0xFFFF	The device ID in the PCIe configuration space is dictated by the device SKU.

Device ID List

Device ID	SKU Branding Name
0x15FD	I225 Hardware Default - Empty Flash Image (or the NVM configuration loading failed)
0x15F2	Intel(R) Ethernet Controller I225-LM
0x15F3	Intel(R) Ethernet Controller I225-V
0x0D9F	Intel(R) Ethernet Controller I225-IT
0x5502	Intel(R) Ethernet Controller I225-LMvP (Dock)
0x125F	I226 Hardware Default - Empty Flash Image (or the NVM configuration loading failed)
0x125B	Intel(R) Ethernet Controller I226-LM
0x125C	Intel(R) Ethernet Controller I226-V
0x125D	Intel(R) Ethernet Controller I226-IT
0x5503	Intel(R) Ethernet Controller I226-LMvP (Dock)

5.1.1.9 Vendor ID - 0x000E

If the Load Vendor/Device IDs bit in Initialization Control Word 1 EEPROM word is set, this word is read in to initialize the PCIe Vendor ID. The default value is 0x8086.

Note: If a value of 0xFFFF is placed in the Vendor ID EEPROM word, the value in the PCIe Vendor ID register will return to the default 0x8086 value. This functionality is implemented to avoid a system hang situation.

Bits	Field Name	Description
15:0	Vendor ID	If the Load Vendor/Device IDs bit in Initialization Control Word 1 EEPROM word is set, this word initializes the PCIe Vendor ID. Note: If a value of 0xFFFF is placed in the Vendor ID EEPROM word, the value in the PCIe Vendor ID register will return to the default 0x8086 value.

5.1.1.10 Initialization Control Word 2 - 0x000F

Bits	Field Name	Default NVM Value	Description
15	APM PME# Enable	0x0	Initial value of the Assert PME On APM Wakeup bit in the Wake Up Control (WUC.APMPME) register.
14	Reserved	0x0	
13:12	Reserved	0x0	
11	Reserved	0x0	
10	FRCSPD	0x0	Default setting for the Force Speed bit in the Device Control register (CTRL[11]).
9	FD	0x1	Default setting for duplex setting. Mapped to CTRL[0].
8	TX_LPI_EN	0x1	Enable entry into EEE LPI on TX path. 0b - Disable entry into EEE LPI on TX path. 1b - Enable entry into EEE LPI on TX path.
7	Reserved	0x0	Reserved zero.
6	PHY Power Down	0x1	When set, the Internal PHY enters a low-power state. This bit is mapped to CTRL_EXT[20]
5	Reserved	0x0	Reserved
4	Reserved	0x0	
3	Reserved	0x0	Reserved zero.
2	EEE_2_5G_AN	0x1	Report EEE 2.5G capability in Auto-negotiation. 0b - Do not report EEE 2.5G capability in Auto-negotiation. 1b - Report EEE 2.5G capability in Auto-negotiation.
1	EEE_1G_AN	0x1	Report EEE 1G capability in Auto-negotiation. 0b - Do not report EEE 1G capability in Auto-negotiation. 1b - Report EEE 1G capability in Auto-negotiation.
0	EEE_100M_AN	0x1	Report EEE 100M capability in Auto-negotiation. 0b - Do not report EEE 100M capability in Auto-negotiation. 1b - Report EEE 100M capability in Auto-negotiation.

5.1.1.11 EEPROM Sizing and Protected Fields - 0x0012

Provides indication on EEPROM size and protection. If the Enable Protection Bit in this word is set and the signature is valid, the software device driver has read but no write access to this word via the EEC and EERD registers; In this case, write access is possible only via an authenticated firmware interface.

Bits	Field Name	Default NVM Value	Description
15:14	Signature	0x1	The Signature field indicates to the device that there is a valid EEPROM present. If the signature field is 01b, EEPROM read is performed, otherwise the other bits in this word are ignored, no further EEPROM read is performed, and default values are used for the configuration space IDs.
13	Security Enabled	0x0	
12	PI Features Enabled	0x0	This bit controls the Printing and Imaging features embedded in FW code.
11	Reserved	0x0	
10:0	Start of 2nd protected area	0x7f0	0x7ff - Means there is no 2nd secured area in the Shadow RAM.

5.1.1.12 LED 1 Configuration Defaults - 0x001C

Bits	Field Name	Description
15:11	Reserved	Reserved
10:8	TXAMP	
7	LED1 Blink	Initial value of LED1_BLINK field.0b = Non- blinking.
6	LED1 Invert	Initial value of LED1_IVRT field. 0b = Active-low output.
5:4	Reserved	Reserved
3:0	LED1 Mode	Initial value of the LED1_MODE field specifying what event/state/pattern is displayed on LED1 (ACTIVITY) output. A value of 0011b (0x3) indicates the ACTIVITY state.

Link Mode Encoding

LEDx_MODE (x=0...3)	LED Functionality
0x0	LED_ON - Always high (Asserted)
0x1	LED_OFF - Always low (De-asserted)
0x2	LINK_UP - Asserted when any speed link is established
0x3	FILTER_ACTIVITY - Asserted when link is established and packets are being transmitted or received that passed MAC filtering
0x4	LINK_ACTIVITY - Asserted when link is established and when there is no transmit or receive activity. When BLINK is set, the LED is on if there is link and it blinks for activity (either receive or transmit).
0x5	LINK_10 - Asserted when a 10 Mb/s link is established
0x6	LINK_100 - Asserted when a 100 Mb/s link is established
0x7	LINK_1000 - Asserted when a 1000 Mb/s link is established
0x8	LINK_2500 - Asserted when a 2500 Mb/s link is established
0x9	SDP_MODE - The SDP pin functions as an SDP. SDP0...2 on LED 0...2 pins respectively.
0xA	PAUSED - Asserted when the transmitter is PAUSED by the flow scheme
0xB	ACTIVITY - Asserted when link is established and packets are being transmitted or received
0xC	LINK_10/100 - Asserted when either 10 or 100 Mb/s link is established
0xD	LINK_100/1000 - Asserted when either 100 or 1000 Mb/s link is established and maintained
0xE	LINK_1000/2500 - Asserted when either 1000 or 2500 Mb/s link is established
0xF	LINK_100/2500 - Asserted when either 100 or 2500 Mb/s link is established and maintained
The dynamic LED modes (FILTER_ACTIVITY, LINK/ACTIVITY, ACTIVITY, PAUSED) should be used with LED Blink mode enabled.	

5.1.1.13 LED 0,2 Configuration Defaults - 0x001F

Bits	Field Name	Description
15	LED2 Blink	Initial value of LED2_BLINK field. 0b = Non-blinking.
14	LED2 Invert	Initial value of LED2_IVRT field. 0b = Active-low output.
13:12	Reserved	Reserved
11:8	LED2 Mode	Initial value of the LED2_MODE field specifying what event/state/pattern is displayed on LED2 (LINK_100) output. A value of 0110b (0x6) indicates 100 Mb/s operation.
7	LED0 Blink	Initial value of LED0_BLINK field. 0b = Non-blinking.
6	LED0 Invert	Initial value of LED0_IVRT field. 0b = Active-low output.
5	Global Blink Mode	Global Blink Mode 0b = Blink at 200 ms on and 200ms off. 1b = Blink at 83 ms on and 83 ms off.
4	Reserved	Reserved. Set to 0b.
3:0	LED0 Mode	Initial value of the LED0_MODE field specifying what event/state/patternis displayed on LED0 (LINK_UP) output. A value of 0010b (0x2) indicates the LINK_UP state.

Link Mode Encoding

LEDx_MODE (x=0...3)	LED Functionality
0x0	LED_ON - Always high (Asserted)
0x1	LED_OFF - Always low (De-asserted)
0x2	LINK_UP - Asserted when any speed link is established
0x3	FILTER_ACTIVITY - Asserted when link is established and packets are being transmitted or received that passed MAC filtering
0x4	LINK_ACTIVITY - Asserted when link is established and when there is no transmit or receive activity. When BLINK is set, the LED is on if there is link and it blinks for activity (either receive or transmit).
0x5	LINK_10 - Asserted when a 10 Mb/s link is established
0x6	LINK_100 - Asserted when a 100 Mb/s link is established
0x7	LINK_1000 - Asserted when a 1000 Mb/s link is established
0x8	LINK_2500 - Asserted when a 2500 Mb/s link is established
0x9	SDP_MODE - The SDP pin functions as an SDP. SDP0...2 on LED 0...2 pins respectively.
0xA	PAUSED - Asserted when the transmitter is PAUSED by the flow scheme
0xB	ACTIVITY - Asserted when link is established and packets are being transmitted or received
0xC	LINK_10/100 - Asserted when either 10 or 100 Mb/s link is established
0xD	LINK_100/1000 - Asserted when either 100 or 1000 Mb/s link is established and maintained
0xE	LINK_1000/2500 - Asserted when either 1000 or 2500 Mb/s link is established
0xF	LINK_100/2500 - Asserted when either 100 or 2500 Mb/s link is established and maintained
The dynamic LED modes (FILTER_ACTIVITY, LINK/ACTIVITY, ACTIVITY, PAUSED) should be used with LED Blink mode enabled.	

5.1.1.14 LAN Power Consumption - 0x0022

Bits	Field Name	Default NVM Value	Description
15:8	LAN D0 Power	0x0	The value in this field is reflected in the PCI Power Management Data Register of the LAN functions for D0 power consumption and dissipation (Data_Select = 0 or 4). Power is defined in 100mW units. The power includes also the external logic required for the LAN function.
7:5	PCIe Function Common Power	0x0	The value in this field is reflected in the PCI Power Management Data register of function 0 when the Data_Select field is set to 8 (common function). The MSBs in the data register that reflects the power values are padded with zeros.
4:0	LAN D3 Power	0x0	The value in this field is reflected in the PCI Power Management Data register of the LAN functions for D3 power consumption and dissipation (Data_Select = 3 or 7). Power is defined in 100 mW units. The power also includes the external logic required for the LAN function. The MSBs in the data register that reflects the power values are padded with zeros.

5.1.1.15 Setup Options PCI Function - 0x0030

The boot agent software configuration is controlled by the NVM with the main setup options stored in word 0x30. These options can be changed by using Control-S setup menu, or by using the IBA Intel Boot Agent Utility.

Note: These settings apply only to Boot Agent software.

Bits	Field Name	Default NVM Value	Description
15:13	RFU	0x0	Reserved. Must be 0.
12:10	FSD	0x0	Bits 12-10 control forcing speed and duplex during driver operation. Valid values are: 0x0 Auto-negotiate 0x1 10 Mb/s Half Duplex 0x2 100 Mb/s Half Duplex 0x3 3 Not valid (treated as 000b) 0x4 4 Not valid (treated as 000b) 0x5 5 10 Mb/s Full Duplex 0x6 6 10 Mb/s Full Duplex 0x7 1000 Mb/s Full Duplex
9	RFU	0x0	
8	DSM	0x1	Display Setup Message. If the bit is set to 1, the "Press Control-S" message is displayed after the title message. Default value is 1.
7:6	PT	0x0	Prompt Time. These bits control how long the CTRL-S setup prompt message is displayed, if enabled by DIM Valid values are: 0x0 2 seconds (default) 0x1 3 seconds 0x2 5 seconds 0x3 0 seconds
5	DEP	0x0	Deprecated. Must be 0.
4:3	DBS	0x0	Default Boot Selection. These bits select which device is the default boot device. These bits are only used if the agent detects that the BIOS does not support boot order selection or if the MODE field of word 31h is set to MODE_LEGACY. Valid values are: 0x0 Network boot, then local boot 0x1 Local boot, then network boot 0x2 Network boot only 0x3 Local boot only
2:0	PS	0x0	Protocol Select. Valid values are: 0x0 PXE enabled 0x1 PXE disabled, possible iSCSI boot 0x2 Primary iSCSI Boot 0x3 Secondary iSCSI Boot Else Reserved

5.1.1.16 PXE Version - 0x0032

When the Boot Agent loads, it can check this value to determine if any first-time configuration needs to be performed. The agent then updates this word with its version. Some diagnostic tools to report the version of the Boot Agent in the flash also read this word.

Bits	Field Name	Default NVM Value	Description
15:12	MAJ	0x1	PXE Boot Agent Major Version. Default value is 0.
11:8	MIN	0x3	PXE Boot Agent Minor Version. Default value is 0.
7:0	BLD	0x32	PXE Boot Agent Build Number. Default value is 0.

5.1.1.17 IBA Capabilities - 0x0033

This word is used to enumerate the boot technologies that have been programmed into the flash. This is updated by flash configuration tools and is not updated or read by IBA.

Bits	Field Name	Default NVM Value	Description
15:14	SIG	0x1	Signature. Must be set to 01 to indicate that this word has been programmed by the agent or other configuration software.
13:4	RFU	0x0	Reserved. Must be 0.
3	UEFI	0x0	UEFI UNDI driver is present in flash if set to 1.
2	RPL	0x0	RPL module is present in flash if set to 1.
1	UNDI	0x1	PXE UNDI driver is present in flash if set to 1.
0	BC	0x1	PXE Base Code is present in flash if set to 1.

5.1.1.18 Checksum Word - 0x003F

Bits	Field Name	Default NVM Value	Description
15:0	Checksum Word	0x0	The checksum words (Offset 0x3F from start of Common, LAN 1, LAN 2 and LAN 3 sections) are used to ensure that the base EEPROM image is a valid image. The value of this word should be calculated such that after adding all the words (0x00:0x3E), including the checksum word itself, the sum should be 0xBABA. The initial value in the 16-bit summing register should be 0x0000 and the carry bit should be ignored after each addition. Note: Hardware does not calculate the checksum word during EEPROM write; it must be calculated by software independently and included in the EEPROM write data. Hardware does not compute a checksum over words 0x00:0x3F during EEPROM reads in order to determine validity of the EEPROM image; this field is provided strictly for software verification of EEPROM validity. All hardware configurations based on word 0x00:0x3F content is based on the validity of the Signature field of the EEPROM Sizing & Protected Fields EEPROM word (Signature must be 01b).

5.1.1.19 PCIe L1 Substates Capability Low - 0x0044

Bits	Field Name	Default NVM Value	Description
15:8	Tcommon-Mode	0x37	Time (in us) required for this Port to re-establish common mode (0-255 us), when exiting L1.2.
7:5	Reserved	0x0	
4	L1 PM Substates Supported	0x1	This bit is loaded to the "L1 PM Substates Supported" bit field in the "L1 PM Sub states Capabilities Register" register in the PCIe configuration space.
3	ASPM L1.1 Supported	0x1	This bit is loaded to the "ASPM L1.1 Supported" bit field in the "L1 PM Sub states Capabilities Register" register in the PCIe configuration space.
2	ASPM L1.2 Supported	0x1	This bit is loaded to the "ASPM L1.2 Supported" bit field in the "L1 PM Sub states Capabilities Register" register in the PCIe configuration space.
1	PCI-PM L1.1 Supported	0x1	This bit is loaded to the "PCI-PM L1.1 Supported" bit field in the "L1 PM Sub states Capabilities Register" register in the PCIe configuration space.
0	PCI-PM L1.2 Supported	0x1	This bit is loaded to the "PCI-PM L1.2 Supported" bit field in the "L1 PM Sub states Capabilities Register" register in the PCIe configuration space.

5.1.1.20 PCIe L1 Substates Capability High - 0x0045

Bits	Field Name	Default NVM Value	Description
15	L1 Substate Enable	1	Expose the L1 substates capability structure in the PCIe configuration space
14:8	Reserved	0x0	
7:3	Port T_POWER_ON Value	0x9	The time (in us) that is requires from the PCIe link partner to wait in L1.2. Exit after sampling CLKREQ# before actively driving the interface. The wait time equals to "Port T_POWER_ON" multiplied by the "Port T_POWER_ON Scale".
2	Reserved	0x0	
1:0	Port T_POWER_ON Scale	0x0	Specifies the scale for the "Port T_POWER_ON Value" as follows: 00b = 2 us 01b = 10 us 10b = 100 us 11b = Reserved

5.1.1.21 PCIe L1 Substates Control 1st Low - 0x0046

Bits	Field Name	Default NVM Value	Description
15:8	Common Mode Restore Time	0x0	
7:4	Reserved	0x0	
3	ASPM L1.1 Enable	0x0	
2	ASPM L1.2 Enable	0x0	
1	PCI-PM L1.1 Enable	0x0	
0	PCI-PM L1.2 Enable	0x0	

5.1.1.22 ULP Capability Enable - 0x004B

Bits	Field Name	Default NVM Value	Description
15	ULP_EN_DevOff	0x1	Enable Ultra Low Power state mode of operation by the DEV_OFF_n signal.
14	ULP_EN_Dr	0x1	Enable Ultra Low Power state mode of operation at dynamic Dr state.
13	ENGY_Wake_DevOff	0x0	Wake on link energy in ULP state triggered by the DEV_OFF_n signal. 0b - Wake on Link Energy is inactive 1b - Wake on Link Energy is active
12	PDown_EN_DevOff	0x1	Enable PHY power down by the DEV_OFF_n signal.
11	PDown_EN_Dr	0x1	Enable PHY power down in Dr state when link is not needed.
10:8	Reserved	0x7	Reserved
7:4	Reserved	0xF	Reserved
3:2	Reserved	0x3	Reserved
1:0	ULP_Delay	0x2	Delay from PE_RST_N driven low till ULP is activated. The delay is defined in seconds units.

6.0 802.1Q VLAN Support

6.1 Overview

The I225/I226 provides several specific mechanisms to support 802.1Q VLANs:

- Optional adding (for transmits) and stripping (for receives) of IEEE 802.1Q VLAN tags.
- Optional ability to filter packets belonging to certain 802.1Q VLANs.
- Double VLAN Support.

6.2 802.1Q VLAN Packet Format

The following diagram compares an untagged 802.3 Ethernet packet with an 802.1Q VLAN tagged packet:

Table 6-1. Comparing Packets

802.3 Packet	#Octets
DA	6
SA	6
Type/Length	2
Data	46-1500
CRC	4

802.1Q VLAN Packet	#Octets
DA	6
SA	6
802.1Q Tag	4
Type/Length	2
Data	46-1500
CRC*	4

Note: The CRC for the 802.1Q tagged frame is re-computed, so that it covers the entire tagged frame including the 802.1Q tag header. Also, max frame size for an 802.1Q VLAN packet is 1522 octets as opposed to 1518 octets for a normal 802.3z Ethernet packet.

6.3 802.1Q Tagged Frames

For 802.1Q, the *Tag Header* field consists of four octets comprised of the Tag Protocol Identifier (TPID) and Tag Control Information (TCI); each taking 2 octets. The first 16 bits of the tag header makes up the TPID. It contains the “protocol type” which identifies the packet as a valid 802.1Q tagged packet.

The two octets making up the TCI contain three fields:

- User Priority (UP)
- Canonical Form Indicator (CFI). Should be 0b for transmits. For receives, the device has the capability to filter out packets that have this bit set. See the *CFIEN* and *CFI* bits in the*RCTL*.
- VLAN Identifier (VID)

The bit ordering is as follows:

Table 6-2. TCI Bit Ordering

Octet 1								Octet 2							
UP			CFI	VID											

6.4 Transmitting and Receiving 802.1Q Packets

6.4.1 Adding 802.1Q Tags on Transmits

Software might command the I225/I226 to insert an 802.1Q VLAN tag on a per packet or per flow basis. If the *VLE* bit in the transmit descriptor is set to 1b, then the I225/I226 inserts a VLAN tag into the packet that it transmits over the wire. 802.1Q tag insertion is done in different ways for legacy and advanced Tx descriptors:

- Legacy Transmit Descriptors: The Tag Control Information (TCI) of the 802.1Q tag comes from the *VLAN* field of the descriptor.
- Advanced Transmit Descriptor: The Tag Control Information (TCI) of the 802.1Q tag comes from the VLAN *Tag* field of the advanced context descriptor. The *IDX* field of the advanced Txdescriptor should be set to the adequate context.

6.4.2 Stripping 802.1Q Tags on Receives

Software might instruct the I225/I226 to strip 802.1Q VLAN tags from received packets. If VLAN stripping is enabled and the incoming packet is an 802.1Q VLAN packet (its *Ethernet Type* field matched the VET), then the I225/I226 strips the 4 byte VLAN tag from the packet, and stores the TCI in the VLAN *Tag* field and the receive descriptor.

The I225/I226 also sets the *VP* bit in the receive descriptor to indicate that the packet had a VLAN tagthat was stripped. If the *CTRL.VME* bit is not set, the 802.1Q packets can still be received if they pass the receive filter, but the VLAN tag is not stripped and the *VP* bit is not set. .

VLAN stripping can be enabled using two different modes:

1. By setting the *DVMOLR.STRVLAN* for the relevant queue.
2. By setting the *CTRL.VME* bit.

6.5 802.1Q VLAN Packet Filtering

VLAN filtering is enabled by setting the *RCTL.VFE* bit to 1b. If enabled, hardware compares the type field of the incoming packet to a 16-bit field in the VLAN Ether Type (VET) register. If the VLAN type field in the incoming packet matches the VET register, the packet is then compared against the VLAN Filter Table Array (VFTA[127:0]) for acceptance.

The I225/I226 provides exact VLAN filtering for VLAN tags for host traffic and VLAN tags for manageability traffic.

6.5.1 Host VLAN Filtering

The *Virtual LAN ID* field indexes a 4096-bit vector. If the indexed bit in the vector is one; there isa Virtual LAN match. Software might set the entire bit vector to ones if the node does notimplement 802.1Q filtering.

In summary, the 4096-bit vector is comprised of 128, 32-bit registers. The *VLAN Identifier (VID)* field consists of 12 bits. The upper 7 bits of this field are decoded to determine the 32-bit register in the VLAN filter table array to address and the lower 5 bits determine which of the 32 bits in the register to evaluate for matching.

6.5.2 Manageability VLAN Filtering

The MC configures the I225/I226 with eight different manageability VIDs via the Management VLAN TAG Value [7:0] - MAVTV[7:0] registers and enables each filter in the MDEF register.

Two other bits in the Receive Control register are also used in conjunction with 802.1Q VLAN filtering operations. CFIEN enables the comparison of the value of the *CFI* bit in the 802.1Q packet to the Receive Control register *CFI* bit as acceptance criteria for the packet.

Note: The VFE bit does not affect whether the VLAN tag is stripped. It only affects whetherthe VLAN packet passes the receive filter.

Table 6-3 lists reception actions per control bit settings.

Table 6-3. Packet Reception Decision

Is Packet 802.1Q?	CTRL.VME	RCTL.VFE	Action
No	X[1]	X[1]	Normal packet reception.
Yes	0b	0b	Receive a VLAN packet if it only passes the standard MAC address filters. Leave the packet as received in the data buffer. The *VP* bit in the receive descriptor is cleared.
Yes	0b	1b	Receive a VLAN packet if it passes the standard filters and the VLAN filter table. Leave the packet as received in the data buffer (the VLAN tag is not stripped). The *VP* bit in the receive descriptor is cleared.
Yes	1b	0b	Receive a VLAN packet if it only passes the standard filters. Strip off the VLAN information (four bytes) from the incoming packet and store in the descriptor. Sets the *VP* bit in the receive descriptor.
Yes	1b	1b	Receive a VLAN packet if it passes the standard filters and the VLAN filter table. Strip off the VLAN information (four bytes) from the incoming packet and store in the descriptor. Sets the *VP* bit in the receive descriptor.

1. X = Don't care.

Note: A packet is defined as a VLAN/802.1Q packet if its *Type* field matches the *VET*.

6.6 Double VLAN Support

The I225/I226 supports a mode where most of the received and sent packet have at least one VLAN tag in addition to the regular tagging which might optionally be added. This mode is used for systems where the switches add an additional tag containing switching information.

Note: The only packets that might not have the additional VLAN are local packets that doesnot have any VLAN tag.

This mode is activated by setting *CTRL_EXT.EXT_VLAN* bit. The default value of this bit is set according to the EXT_VLAN (bit 1) in the *Initialization Control 3* NVM word.

The type of the VLAN tag used for the additional VLAN is defined in the *VET.VET_EXT* field.

6.6.1 Transmit Behavior with External VLAN

It is expected that the driver includes the external VLAN header as part of the transmit data structure. Software might post the internal VLAN header as part of the transmit data structure or embedded in the transmit descriptor. The I225/I226 does not relate to the external VLAN header other than the capability of "skipping" it for parsing of inner fields.

Notes:

- If the *CTRL_EXT.EXT_VLAN* bit is set the VLAN header in a packet that carries asingle VLAN header is treated as the external VLAN.
- If the *CTRL_EXT.EXT_VLAN* bit is set the I225/I226 expects that any transmitted packetto have at least the external VLAN added by the software. For those packets where an external VLAN is not present, any offload that relates to inner fields to the EtherType might not be provided.
- If the regular VLAN is inserted from the descriptor, and the packet does not contain an external VLAN, the packet is dropped, and if configured, the queue from which the packet was sent is disabled.

6.6.2 Receive Behavior With External VLAN

When the I225/I226 is working in this mode, it assumes that all packets received have at least one VLAN, including a packet received or sent on the manageability interface.

One exception to this rule are flow control PAUSE packets which are not expected to have any VLAN. Other packets might contain no VLAN, however a received packet that does not contain the first VLAN is forwarded to the host, but filtering and offloads are not applied to this packet.

See Table 6-4 for the supported receive processing functions when the device is set to "Double VLAN" mode.

Stripping of VLAN is done on the second VLAN if it exists. All the filtering functions of the I225/I226 ignore the first VLAN in this mode.

The presence of a first VLAN tag is indicated it in the *RDESC.STATUS.VEXT* bit.

Queue assignment of the Rx packets is not affected by the external VLAN header. It might depend on the internal VLAN, MAC address or any upper layer content.

Table 6-4. Receive Processing in Double VLAN Mode

VLAN Headers	Status.VEXT	Status.VP	Packet Parsing	Rx Offload Functions
External and internal	1	1	+	+
Internal Only	Not supported			
V-Ext	1	0	+	+
None[1]	0	0	+ (flow control only)	-

1. A few examples for packets that might not carry any VLAN header might be: Flow control and Priority Flow Control; LACP; LLDP; GMRP; 802.1x packets.

7.0 Electrical and Timing Specifications

7.1 Introduction

This section describes the I225/I226 recommended operating conditions, power delivery, DC electrical characteristics, power sequencing and reset requirements, PCIe specifications, reference clock, and packaging information.

7.2 Operating Conditions

7.2.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
$T_{storage}$	Storage Temperature Range	-40	125	°C
T_{ML3}	Moisture Level 3 Temperature Limits (According to IPS J-STD 020)	-	260	°C
3.3V	3.3V Supply Voltage	-0.5	3.63	Vdc
VDD (0.95V)	0.95V Supply Voltage	-0.5	1.0	Vdc

Notes:

1. Ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation. Exposure to absolute maximum rating conditions for extended periods might affect device reliability.
2. Recommended operation conditions require accuracy of power supply of ±5% relative to the nominal voltage.
3. The digital I/O absolute maximum must be no higher than the 3.3V supply pad.
4. Maximum ratings are referenced to ground (VSS).

7.2.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Units
T-AMBIENT (Commercial)	Commercial Operating Temperature Range[1]	0	-	70[2]	°C
T-CASE (Commercial)	Case Temperature Range	0	-	100[2]	°C
Tj (Commercial)	Junction Temperature	0	-	110	°C
T-AMBIENT (Extended Temp[3])	2.5G Extended Operating Temperature Range[1]	-40	-	70[2]	°C
T-AMBIENT (Extended Temp[3])	10M/100M/1G Extended Operating Temperature Range[1]	-40	-	85[2]	°C
T-CASE (Extended Temp[3])	Case Temperature Range	-40	-	100[2]	°C
Tj (Extended Temp[3])	Junction Temperature	-40	-	110	°C
3.3V	3.3V Supply Voltage	3.135	3.3	3.465	Vdc
VDD (0.95V)	VDD (0.95V) Supply Voltage iSVR can vary dynamically (depending on the load) Vripple_max = 60 mV	0.92	0.95	0.98	Vdc
Vid	XTAL1 Input Voltage	-0.3	-	2	V

1. Ambient; 0 CFS airflow
2. For normal device operation, adhere to the limits in this table. Sustained operations of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, can result in permanent device damage or impaired device reliability. Device functionality to stated Vdc and Vac limits is not guaranteed if conditions exceed recommended operating conditions.
3. For I225-IT/I226-IT SKU only.

7.2.3 Power Up Sequence

VDD (0.95V) must power up within 50 ms (power supply setting time) after 3.3 Vdc powers up. After power supply settling time, all primary input signals to the I225/I226 should be defined.

The I225/I226 requires 3.3 Vdc from an external power supply. The I225/I226 has its own VDD, the DC-DC internal Switching Voltage Regulator (iSVR), which is derived internally from its 3.3 Vdc rail.

3.3V ramp up ($t_{33rampup}$) should be at least 50 µs.

3.3V stable to VDD(0.95V) stable (t_{power}) should be less than 50 ms. 3.3V

ramp down ($t_{33rampdown}$) should be at least 1 ms.

The VDD (0.95V) voltage ramp must never be higher than the 3.3V voltage ramp.

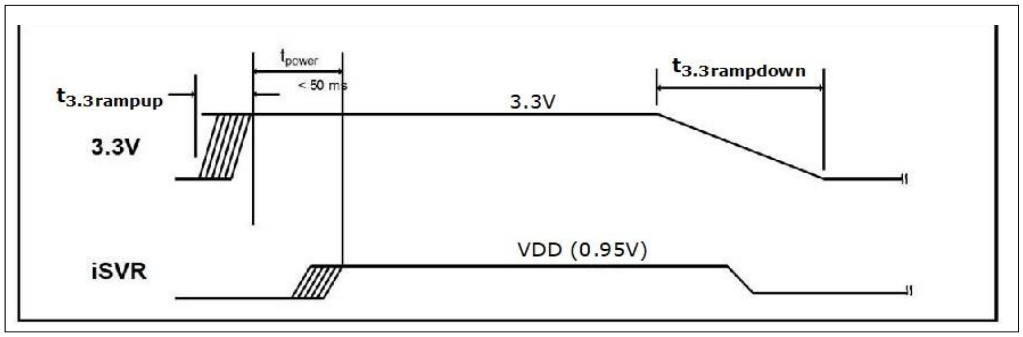

Figure 7-1. Power Up Sequence

7.3 DC Characteristics

7.3.1 GPIO Interface

The DC characteristics of the GPIO interface including the following: SPI, Clock outputs, LED, JTAG.

Table 7-1. GPIO Logic Level

Parameter	Minimum	Typical	Maximum	Unit
VIH	2	3.3	3.6	Vdc
VIL	-0.3	0	0.8	Vdc
VOH	2.9	3.3	-	Vdc
VOL	-	0	0.4	Vdc

Table 7-2. GPIO Open Drain

Pin Name	Bus Size	Description
PE_CLKREQ_N	1	Open-drain I/O
SMB_CLK	1	Open-drain I/O
SMB_DATA	1	Open-drain I/O

7.3.2 MDI Twisted Pair Interface

The TPI conforms to the specifications of 10BASE-Te (Clause 14), 100BASE-TX (Clause 25), 1000BASE- T (Clause 40) and 2.5GBASE-T (Clause 126) given in IEEE802.3-2005, IEEE802.3bz, as well as ANSI X3.263-1995.

7.4 AC Characteristics

7.4.1 3.3 Vdc Power Rail

Title	Description	Min	Max	Units
$t_{3.3Vrampup}$	Time from 10% to 90% mark	0.050	50	ms
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Operational Range	Voltage range for normal operating conditions	3.135	3.46	V
Ripple	Maximum voltage ripple (peak to peak)	N/A	100	mV
Overshoot	Maximum overshoot allowed	N/A	100	mV

7.4.2 VDD (0.95V) iSVR Specification

By using the integrated DC/DC switching regulator, the I225/I226 can be powered using a single power supply of 3.3 Vdc (see Figure 7-2). As long as the applied nominal voltage remains in the operating conditions, the device operates automatically and without the need for additional settings to be applied. Only minor external circuitry is required to enable this feature. The electrical requirements are defined in the AC characteristics of the power supply.

Table 7-3. iSVR Specification

Parameter	Specifications			Units	Comments
	Min	Typ	Max		
DC/DC Inductance		1.0		µH	Imax = 1.2 A
DC/DC Output Capacitance		2x22		µF	**Important:** Put the decoupling capacitors at pin 9 and pin 38. Refer to the *I225/I226 Reference Schematic and the I225/I226 Schematic/ Layout Checklist* for details.
DC/DC Input Capacitance		2x22		µF	**Important:** Put the decoupling capacitors at pin 7. Refer to the *I225/I226 Reference Schematic and the I225/I226 Schematic/ Layout Checklist* for details.
Power supply ripple			60	mV	Peak-to-peak value

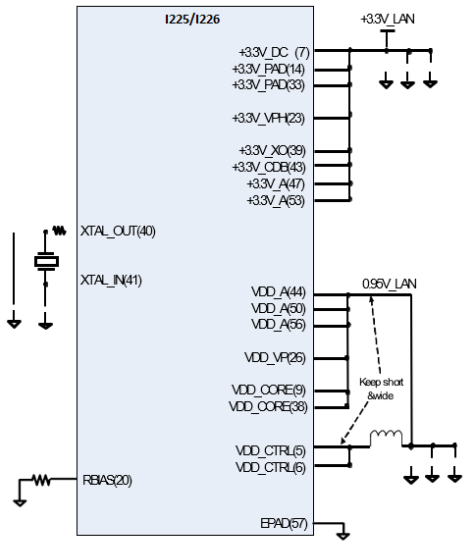

Figure 7-2. Power Delivery Schematic with Integrated SVR

7.4.3 Serial Peripheral Interface SPI Flash

The SPI flash must support page program which allow from 1 to 256 bytes programming at a time.

The SPI master interface timing is shown in Figure 7-3.

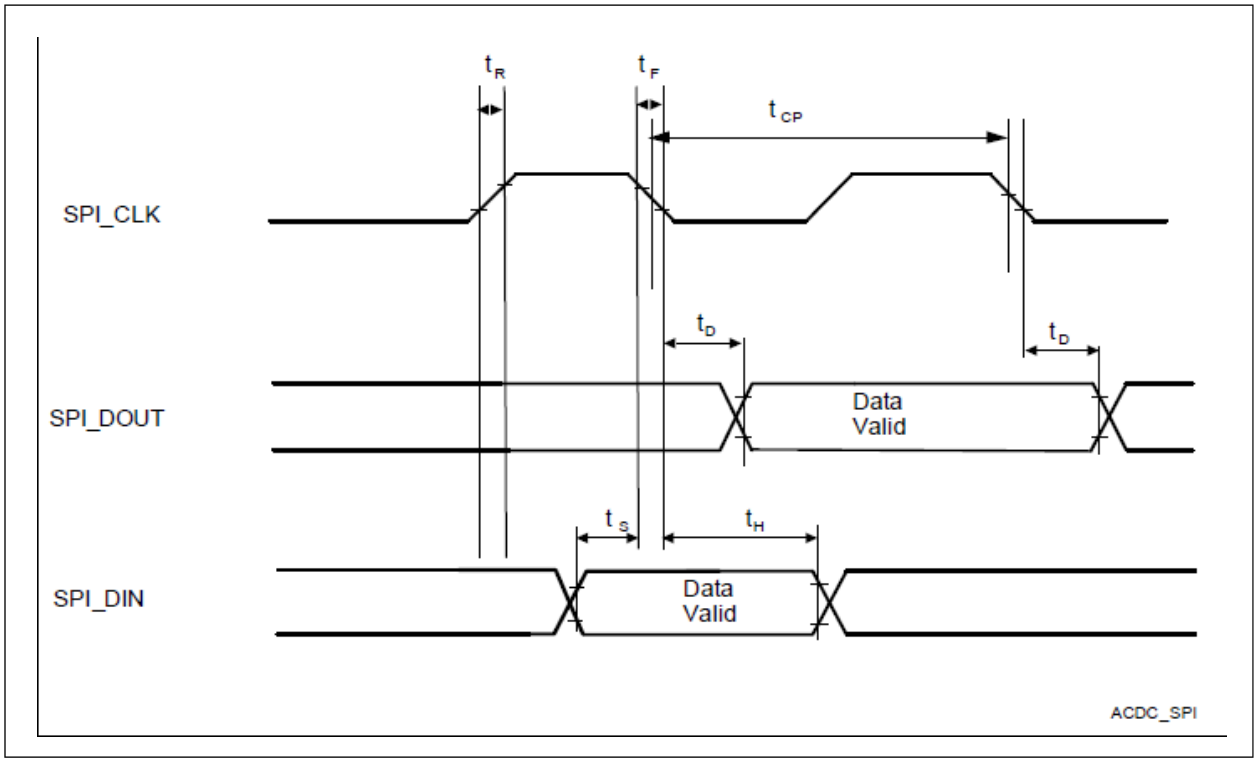

Figure 7-3. SPI Master Interface Timing

Table 7-4. SPI Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min	Typ	Max		
Master Mode						
Tx Data Output Delay	t_D	0	-	4	ns	-
Rx Data Input Setup Time	t_S	7	-	-	ns	-
Rx Data Hold Time	t_H	0	-	-	ns	-
SPI Clock Period (Master Mode)	t_{CP}	20	-	50	ns	
SPI Clock Rise Time	t_R	-	-	5.0	ns	10% - 90%
SPI Clock Fall Time	t_F	-	-	5.0	ns	10% - 90%
SPI Clock Duty Cycle	D	45	-	55	%	-

7.4.4 Crystal Specifications

Table 7-7. External Crystal Specifications

Parameter Name	Symbol	Recommended Value	Max/Min Range	Conditions
Frequency	f_o	25 [MHz]		@ 25 [°C]
Vibration Mode		Fundamental		
Frequency Tolerance @25 °C	Df/f_o @25°C	±30 [ppm]		@ 25 [°C]
Temperature Tolerance	Df/f_o	±30 [ppm]		0 to +70 [°C]
Series Resistance (ESR)	R_s		60 [Ω] max	@ 25 [MHz]
Crystal Load Capacitance	C_{load}	18 [pF]		
Shunt Capacitance	C_o		5 [pF] max	
Drive Level	D_L		100 [µW] max	
Aging	Df/f_o	±5 ppm per year	±5 ppm per year max	
Calibration Mode		Parallel		
Insulation Resistance			500 [MΩ] min	@ 100 Vdc

7.4.5 PCIe Specification

The I225/I226 supports the PCIe Gen 2 v3.1 interface.

For transmit/receive/clock, refer to the standard PCIe specification for requirements.

7.4.6 Discrete/Integrated Magnetics Specifications

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Turns Ratio	1:tr	0.95	1	1.05	%	±5%
Differential-to-Common-Mode Rejection	DCMR	40	-	-	dB	30 MHz
		35	-	-	dB	60 MHz
		30	-	-	dB	100 MHz
Crosstalk Attenuation	CTA	45	-	-	dB	30 MHz
		40	-	-	dB	60 MHz
		35	-	-	dB	100 MHz
Insertion Loss	IL	-	-	1	dB	1 MHz ≤ f ≤ 125 MHz
Return Loss	RL	16	-	-	dB	1 MHz ≤ f ≤ 40 MHz
Return Loss	RL	16-10*log10(f/40)	-	-	dB	40 MHz ≤ f ≤ 125 MHz

7.4.7 RJ45 Plug

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Crosstalk attenuation	CTA	45	-	-	dB	30 MHz
		40	-	-	dB	60 MHz
		35	-	-	dB	100 MHz
Insertion Loss	IL	-	-	1	dB	1 MHz ≤ f ≤ 125 MHz
Return Loss	RL	16	-	-	dB	1 MHz ≤ f ≤ 40 MHz
Return Loss	RL	16-10*log10(f/40)	-	-	dB	40 MHz ≤ f ≤ 125 MHz

7.4.8 Serial Peripheral Interface SPI Flash

The SPI master interface timing is shown in Figure 7-6.

Figure 7-5. SPI Master Interface Timing

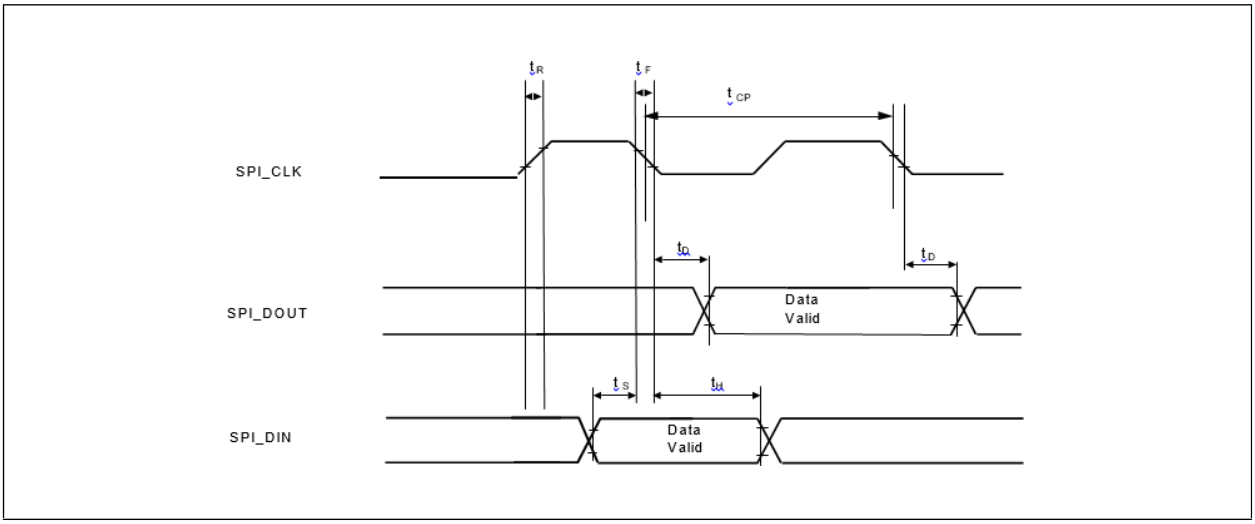

Table 7-8. SPI Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Tx Data Output Delay	t_D	0	–	4	ns	–
Rx Data Input Setup time	t_S	7	–	–	ns	–
Rx Data Hold time	t_H	0	–	–	ns	–
SPI Clock Period (Master Mode)	t_{CP}	10	–	50	ns	–
SPI Clock Rise Time	t_R	–	–	1.0	ns	10% - 90%
SPI Clock Fall Time	t_F	–	–	1.0	ns	10% - 90%
SPI Clock Duty Cycle	D	45	–	55	%	–

7.5 Recommended Component List

The following tables show the parts have been used successfully with I225/I226. Parts listed in the alphabetical order; no particular product has higher priority. These parts should be good candidates as the starting point. All customer designs must have validations for production quality.

Table 7-11. Discrete RJ45 Connector

Manufacturer	Part Number
Matrix	MRJN-11T512TRS[1]
Foxconn	JI51015-SB01-4F
Lotes	ABA-JKM-007-Y01[1]

1. Supports I225-IT/I226-IT extended temperature SKU.

Table 7-12. Discrete Magnetics

Manufacturer	Part Number
Bothhand	QVPR2014R/QVPR2014M[1]
Bothhand	AGST5009/AGST5009M[1]
FPE	LK24121SN LK24123SN
Pulse	H5G1003NL

1. Supports I225-IT/I226-IT extended temperature SKU.

Table 7-13. Integrated Magnetics RJ45 Connector: (Also Called ICM or MagJack)

Manufacturer	Part Number
Pulse	JT4-2504HL
Delta	RCMCU1F2462JRIN[1]

1. Supports I225-IT/I226-IT extended temperature SKU.

Table 7-14. Integrated Magnetics RJ45 + USB Ports

Manufacturer	Part Number
TRP	2250576-2
UDE	RUP-NT-0004
UDE	RUP-NT-0009[1]

1. Supports I225-IT/I226-IT extended temperature SKU.

Table 7-15. Crystal

Manufacturer	Part Number
Hosonic	E3SB25E001802E[1]
TXC	7M25020018(21)[1]

1. Supports I225-IT/I226-IT extended temperature SKU.

Table 7-16. Inductor 1.0uH (for iSVR)

Manufacturer	Part Number
Murata	DFE201610E-1R0M[1]
IDT	SF20121-1R0M[1]

1. Supports I225-IT/I226-IT extended temperature SKU.

Table 7-17. SPI Flash

Manufacturer	Part Number
Macronix	MX25L1606EM1I-12G[1]
Winbond	W25Q16JVSNIQ[1]

1. Supports I225-IT/I226-IT extended temperature SKU.

Table 7-18. EDS/TVS

Manufacturer	Part Number
OnSemi	ESD8708[1]

1. Supports I225-IT/I226-IT extended temperature SKU.

Note: Consult with ESD part vendors for selecting the right component to achieve applicable ESD requirements.

8.0 Package and Order Information

8.1 Introduction

This section describes the I225/I226's package and order information.

8.2 Package Outline

The I225/I226 is assembled in a PG-VQFN-56 package, which complies with regulations requiring lead-free material. See Figure 8-1, Figure 8-4, and Figure 8-3 for package detail. Table 8-1 lists thermal resistance for packaging.

Note: Package dimensions are in millimeters.

Table 8-1. JEDEC Thermal Resistance Package Parameters

Item	Description/Value
Package Type	PG-VQFN-56
Thermal Resistance Junction-to-Ambient (Reference to JEDEC JESD51-2)	$R_{th, JA}$ = 25.9 K/W Psi_{JCTop} = 0.37 K/W Psi_{JB} = 11.7 K/W
Thermal Resistance Junction-to-Case (Reference to JEDEC JESD15-3)	$R_{th, JCtop}$ = 19.8 K/W $R_{th, JB}$ = 11.7 K/W

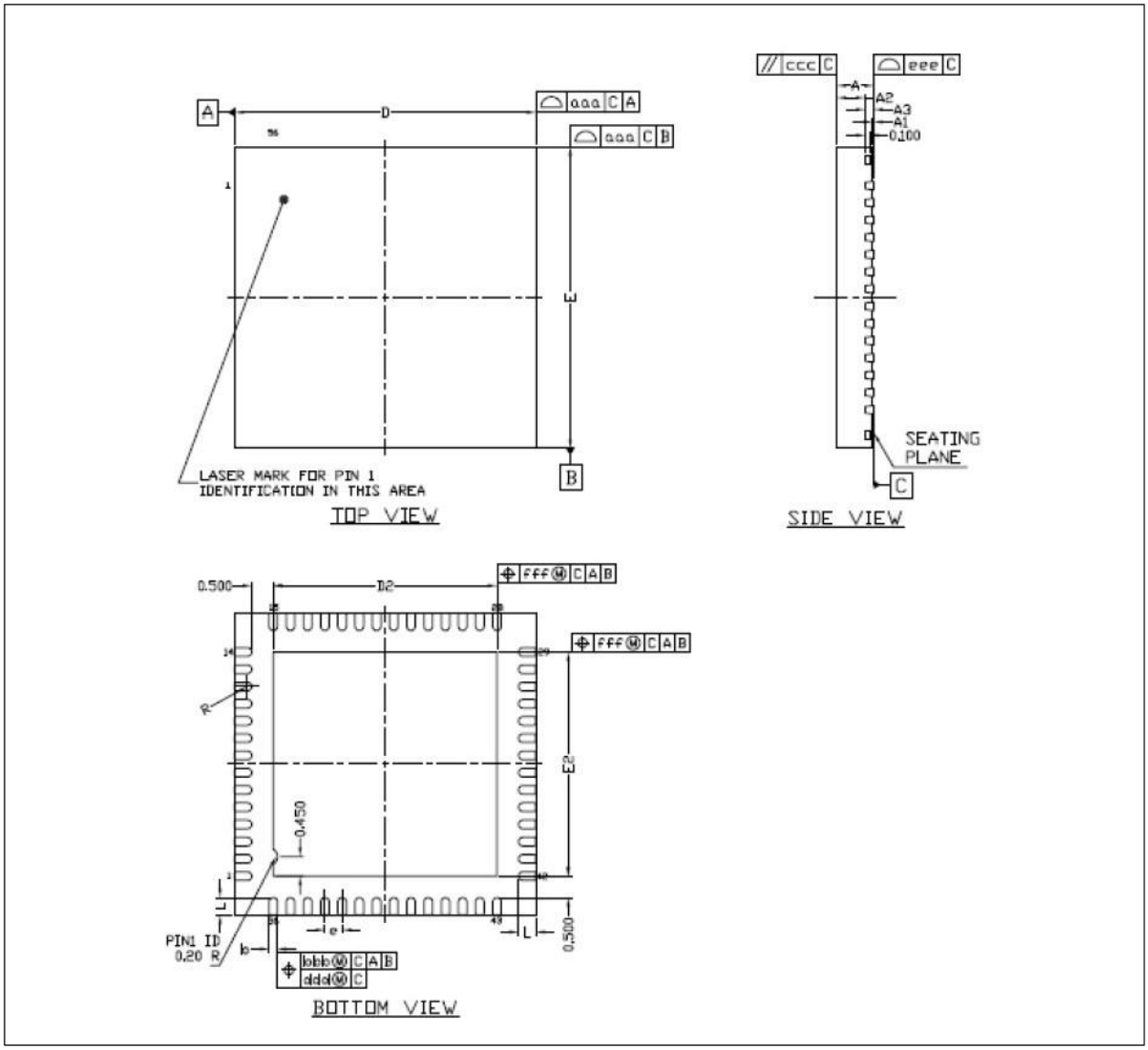

Figure 8-1. Package Outline

Figure 8-4 and Figure 8-5 shows package outline information.

■ CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.900	---	---	0.035
A1	0.000	---	0.050	0.000	---	0.002
A2	---	0.650	0.700	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	7 BSC			0.276 BSC		
D2	5.100	5.200	5.300	0.201	0.205	0.209
E	7 BSC			0.276 BSC		
E2	5.100	5.200	5.300	0.201	0.205	0.209
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.400 BSC			0.016 BSC		
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

Figure 8-2. Package Outline Dimensions

1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

Figure 8-3. Package Outline Notes

8.3 Tape and Reel Carrier Drawing

Figure 8-4 shows the carrier tape package information.

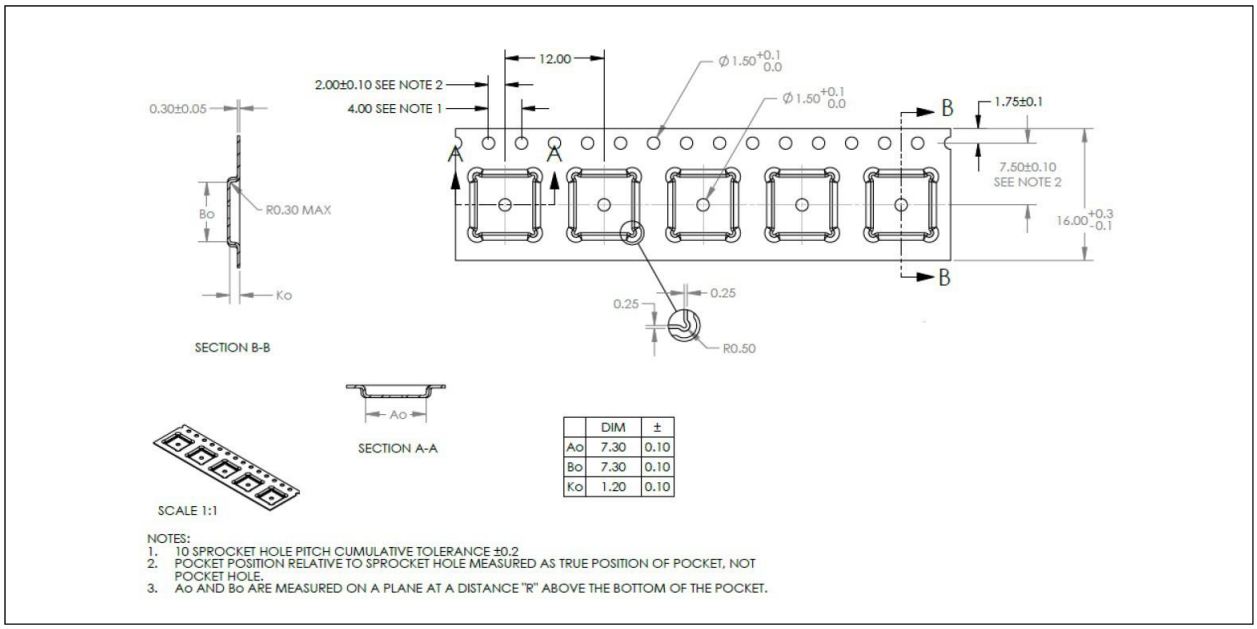

Figure 8-4. Carrier Tape Packing Information

8.4 Pin1 Orientation and Feeding Direction

Figure 8-5 shows the direction of the tape feeding with Pin1 at the top right.

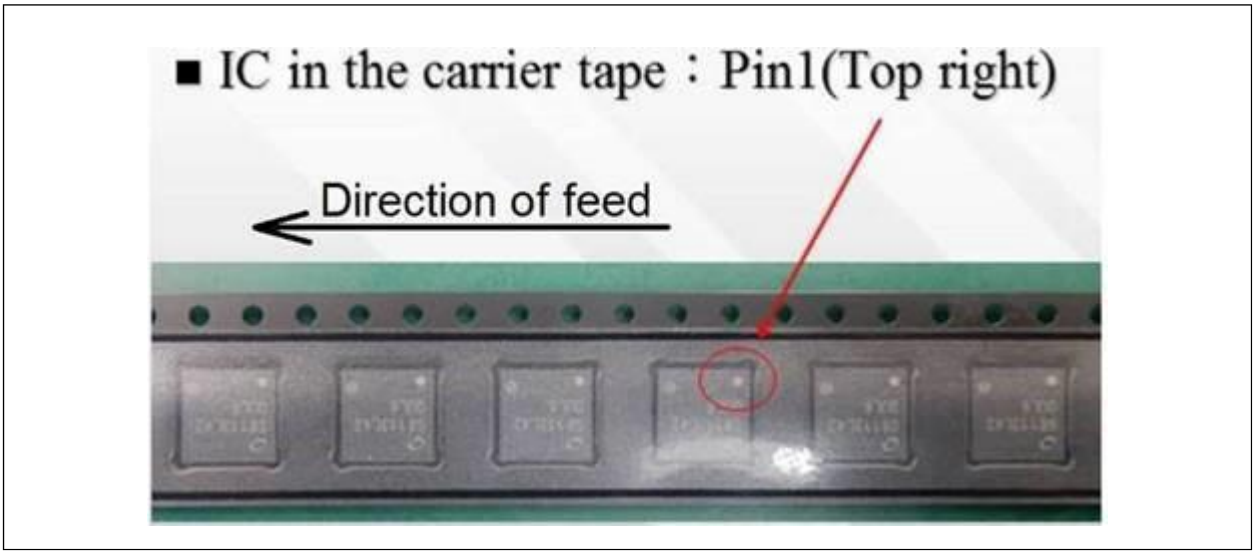

Figure 8-5. Carrier Tape Pin1 Orientation and Feeding Direction

8.5 Tray Drawing

Figure 8-6 and Figure 8-7 show the tray drawing details for manufacturing.

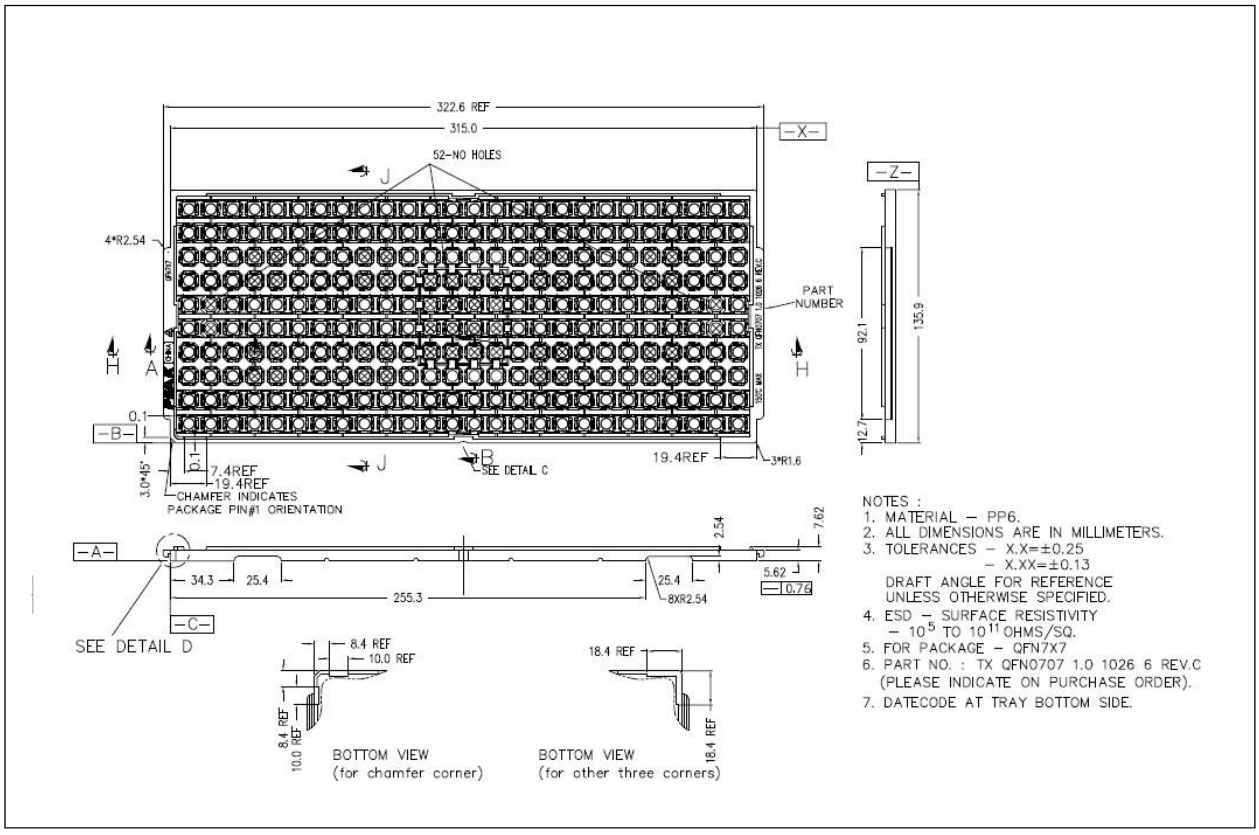

Figure 8-6. Tray Drawing

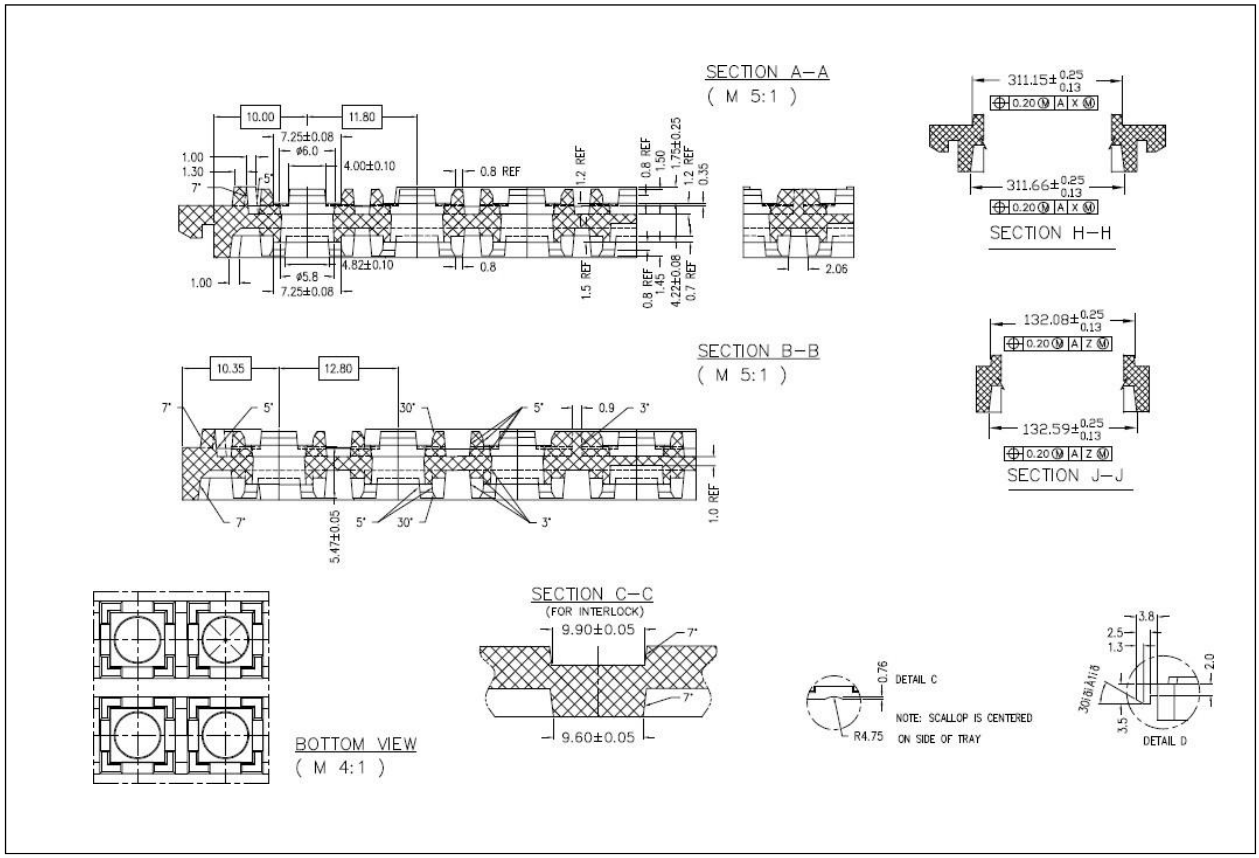

Figure 8-7. Tray Drawing in Detail

8.6 I225/I226 Identification Information

Figure 8-8 and Figure 8-9 show the marking pattern and marking information for the I225/I226.

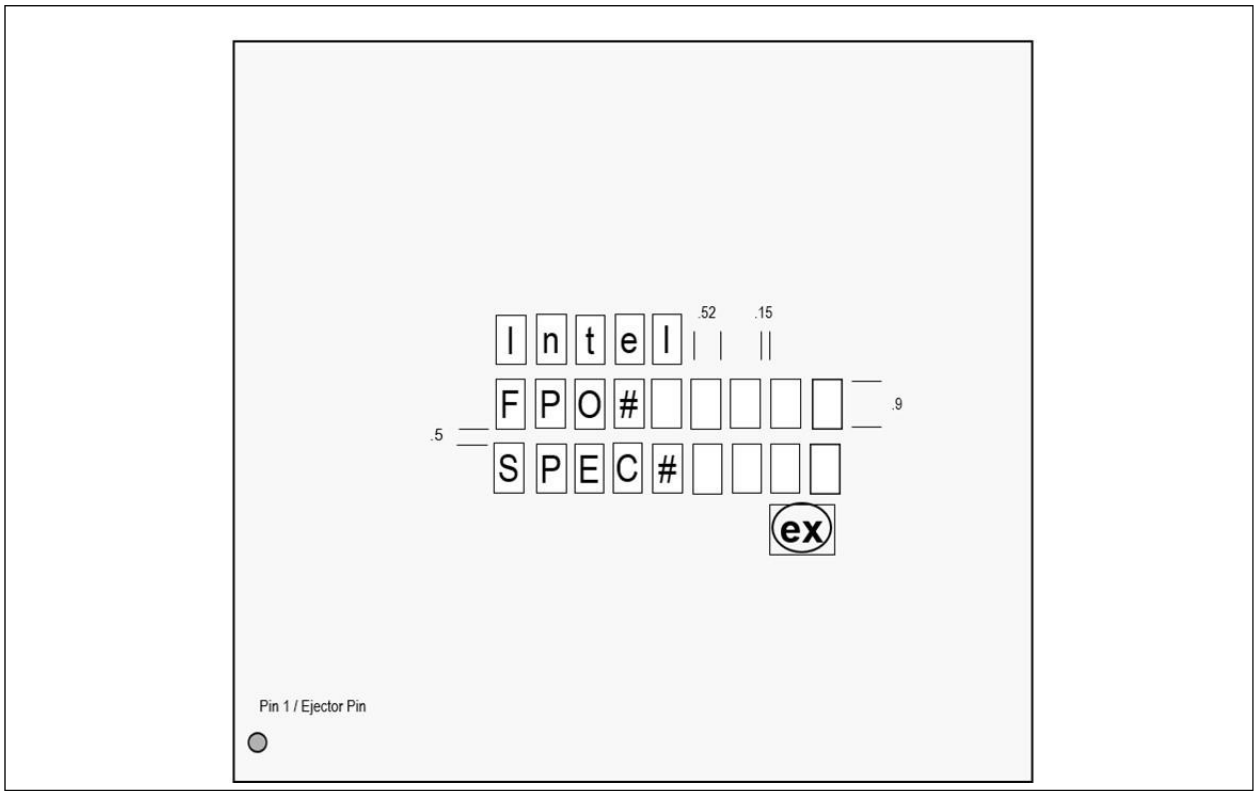

Figure 8-8. I225/I226 Product Identification Marking

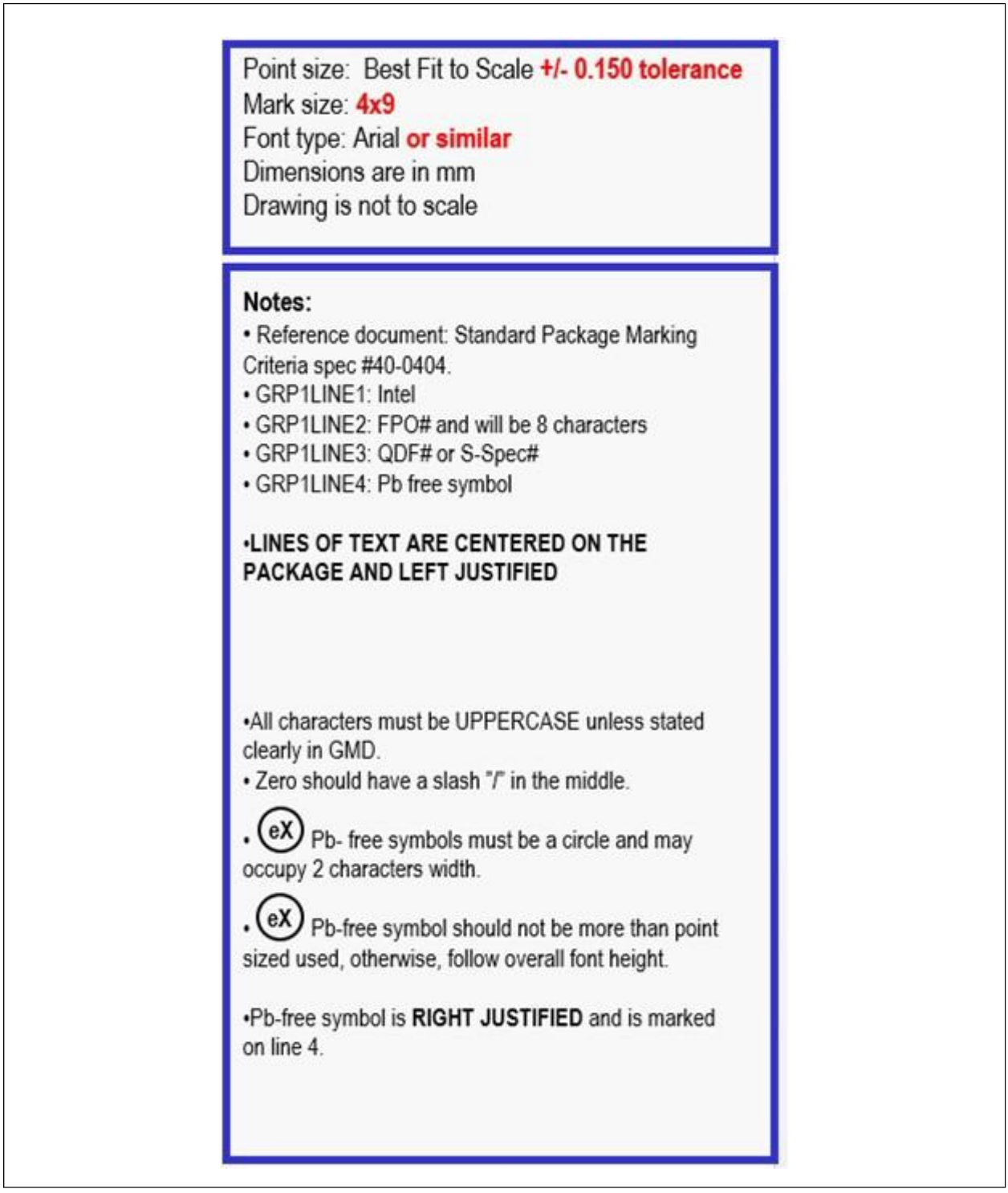

Figure 8-9. Marking Information

8.7 Order Information

For I225/I226 sales ordering information, refer to the Intel Message of The Week Document (Doc#574707) and the table below.

Part #	Step	Intel MM #	Spec Code	Type	Std Pack Qty	Type
I225-LM (Foxville-LM, v3)	B3	99A40V	QVZP	Tray	1	Q-SPEC; preproduction
I225-IT (Foxville-IT, v3)	B3	99A3V4	QVYZ	Tray	1	Q-SPEC; preproduction
I225-LM (Foxville-LM, v3)	B3	99A57P	SLNNJ	T&R	4000	S-SPEC; Production
I225-LM (Foxville-LM, v3)	B3	99A57N	SLNNH	Tray	1	S-SPEC; Production
I225-V (Foxville-V, v3)	B3	99A3W6	SLNMH	T&R	4000	S-SPEC; Production
I225-V (Foxville-V, v3)	B3	99A3W5	SLMNG	Tray	1	S-SPEC; Production
I225-IT (Foxville-IT, v3)	B3	99A57T	SLNNL	T&R	4000	S-SPEC; Production
I225-IT (Foxville-IT, v3)	B3	99A57R	SLNNK	Tray	1	S-SPEC; Production
I226-LM (Foxville-LM C-step)	C	99AA68	QW93	Tray	1	Q-SPEC; preproduction
I226-IT (Foxville-IT C-step)	C	99AFN5	SRKTX	Tray	1	S-SPEC; Production
I226-IT (Foxville-IT C-step)	C	99AFN4	SRKTW	T&R	4000	S-SPEC; Production
I226-LM (Foxville-LM C-step)	C	99AFMX	SRKTT	Tray	1	S-SPEC; Production
I226-LM (Foxville-LM C-step)	C	99AFMW	SRKTS	T&R	4000	S-SPEC; Production
I226-V (Foxville-V C-step)	C	99AFN3	SRKTV	Tray	1	S-SPEC; Production
I226-V (Foxville-V C-step)	C	99AFN0	SRKTU	T&R	4000	S-SPEC; Production

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