AC7026A2 Datasheet

Zhuhai Jieli Technology Co.,LTD

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AC7026A2 Features

CPU

- 32-bit DSP
- with IEEE754 Single precision FPU
- Mathematic alaccelerate engine
- Up to 160MHz programmable processor
- 16KB Icache and 2KB Dcache (read only)
- 64Vectored interrupts
- 8 Levels interrupt priority

Memory

- On-chip 132KB SRAM (include cache)
- On-chip 544KB ROM
- Support MMU
- Built-In Flash
- 4 region MPU protects

Clocks

- On-chip 16 MHz clock oscillator
- On-chip 200 kHz lower-temperature-drift clock oscillator
- 24 MHz crystal oscillator

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Packet Loss Concealment (PLC) for voice processing
- Single MIC Environmental Noise Cancellation (ENC)
- Single-band DRC limiter
- Multi-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC,SNR ≥ 102dB
- One channels 16-bit ADC,SNR ≥ 90dB
- Audio DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/ 32kHz/44.1kHz/48kHz/64kHz/88.2kHz/ 96kHz are supported
- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32 kHz/44.1kHz/48kHz are supported
- Support four digital/analog MIC inputs
- One channels analog audio inputs
- Audio DAC supports differential cap-less mode or single-ended mode
- Direct drive 16ohm/32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V5.3+BR+EDR+BLE specification
- Meet class2 and class3 transmitting power requirement
- Maximum +8dbm transmitting power
- EDR receiver with -94dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\ att\gap\gatt\rfcomm\sdp\l2cap profile
- a2dp 1.3.2\avctp 1.4\avdtp 1.3\ avrcp 1.6.2\hfp 1.8 \spp 1.2\rfcomm 1.1\pnp 1.3\hid 1.1.1\sdp core5.3\l2cap core 5.3

Peripherals

- One full speed USB OTG controller
- One SD host controller for eMMC/SD
- Six multi-function 32-bit timers, support capture and PWM mode
- Four UART interface, UART0,UART1&UART2 support DMA
- I2C Master/Slave interface
- SPI Master/Slave interface
- I2S Master/Slave interface
- QDEC
- Low power CapSense
- 13-channel 10-bit ADC for analog sampling
- 16 Individually programmable and multiplexed GPIO pins
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

PMU

- Built-in lithium battery charging manager,up to 200mA charging current
- Built-in LDO and Buck DC-DC converter
- 3uA current consumption in the soft-off mode
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.7V to 4.5V
- IOVDD range : 2.0V to 3.4V

Packages

- QFN32(4mm*4mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Bluetooth Stereo Headsets and Headphones
- Bluetooth TWS ANC Earphones
- Bluetooth Stereo ANC Headsets and Headphones

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1 Block Diagram

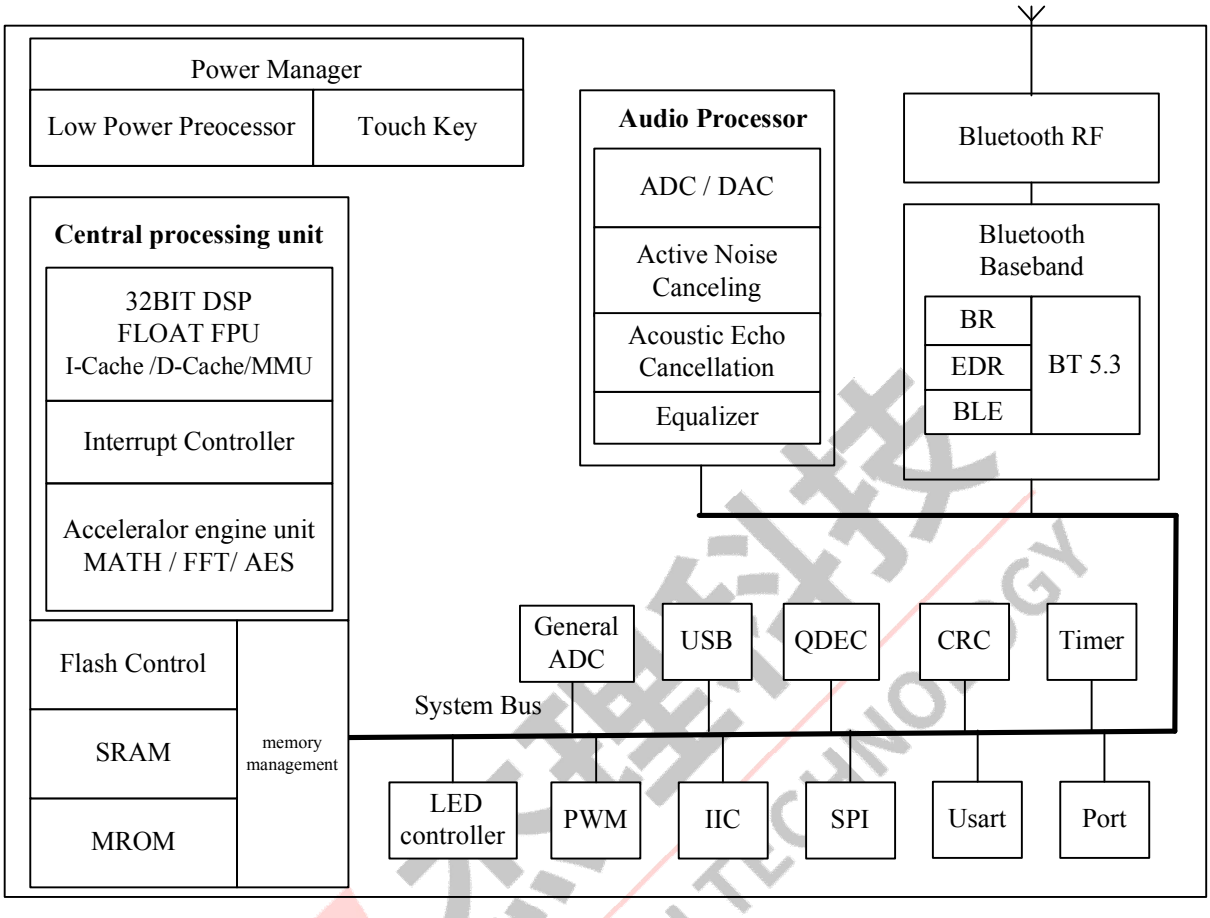


Figure 1-1 AC7026A Block Diagram

2 Pin Definition

2.1 Pin Assignment

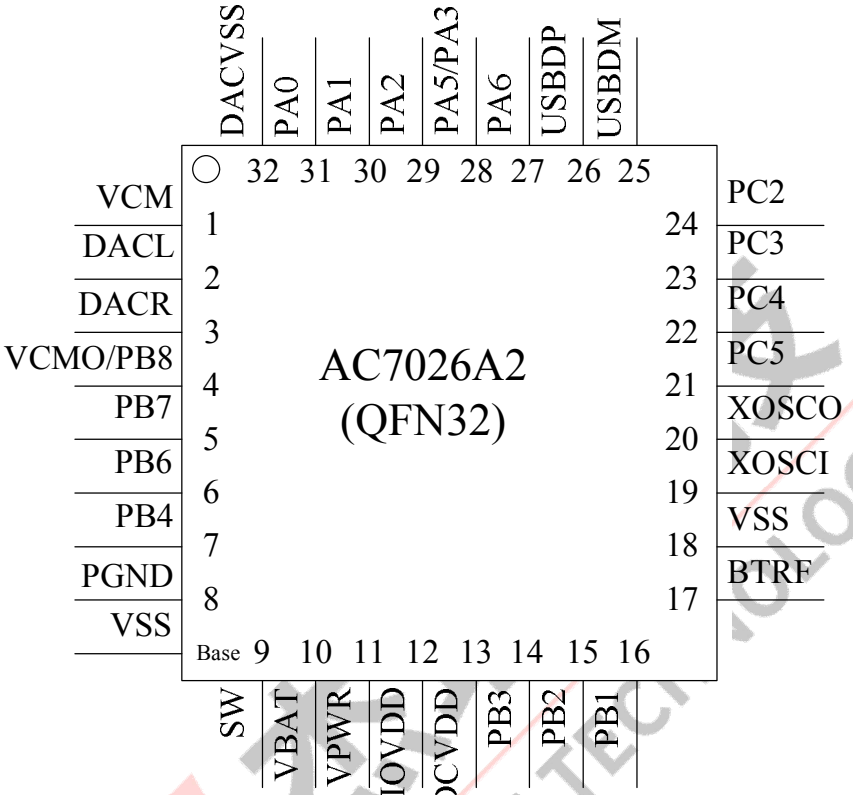


Figure 2-1 AC7026A Package Diagram

2.2 Pin Description

Table 2-1 AC7026A Pin Description

Pin No.	Pin name	Type	Function	Other function
1	VCM	P		Audio analog reference bias;
2	DACL	AO	Analog Output	Left channel audio output positive;
3	DACR	AO	Analog Output	Right channel audio output positive;
4	VCMO	P		-
	PB8	I/O	GPIO	UART0RXB :Uart0 Data In(B); CAP4: Timer4 Capture;
5	PB7	I/O	GPIO	SPI1DOA : SPI1 Data Out(A); Q-decoder1: quadrature decoder 1; ADC8 :ADC Input Channel 8; UART0TXB :Uart0 Data Out(B); TMR5 : Timer5 Clock In;
6	PB6	I/O	GPIO	SPI1CLKA: SPI1 Clock(A); Q-decoder0 : quadrature decoder 0; ADC9 :ADC Input Channel 9; UART1RXA :Uart1 Data In(A); PWM2 :Timer2 PWM Output;
7	PB4	I/O	GPIO	CLKOUT0：Clock Out0; LVD; SPI0_DAT2A(2); SPI1DIA :SPI1 Data In(A); SFC_DAT2A(2); ADC12 :ADC Input Channel 12; UART1TXA :Uart1 Data Out(A); TMR2 :Timer2 Clock In;
8	PGND	G		The ground of Buck DC-DC converter;
9	SW	PO		Switch signal of the Buck converter, connected to inductor;
10	VBAT	PI	GPIO	Battery interface;
11	VPWR (PP0)	PI (I/O)	GPIO (High Voltage Input)	Charge Power Input; UART0TXC：Uart0 Data Output(C); UART0RXC：Uart0 Data Input(C); PWM3：Timer3 PWM Output； CAP1：Timer1 Capture;
12	IOVDD	PO		IO Power;
13	DCVDD	P		DCDC power 1.25V;

14	PB3	I/O	GPIO	EVDD/PVDD ; SPI2DIC : SPI Data In(C); ALNK_MCLKB : Audio Link Main Clk(B); ADC7: ADC Input Channel 7; UART1TXB/UART1RXB: Uart1 Data Out(B); TMR4: Timer4 Clock In;
15	PB2	I/O	GPIO	LP_Touch1 :Low Power Touch Channel 1; SPI2DOC:SPI Data Out(C); UART2RXC: Uart2 Data In(C); CAP5: Timer5 Capture;
16	PB1	I/O	GPIO	LP_Touch0 :Low Power Touch Channel 0; SPI2CLKC : SPI2 Clock(C); UART2TXC :Uart2 Data Out(C); TMR0 :Timer0 Clock In;
17	BTRF	RFI		Bluetooth RF antenna interface;
18	VSS	G		Ground;
19	XOSCI	I		System Crystal Oscillator Input;
20	XOSCO	O		System Crystal Oscillator Output;
21	PC5	I/O	GPIO	SPI1DOB: SPI1 Data Out(B); IIC_SDA_B : IIC Data(B); ALNK_DAT3B : Audio Link Data3(B); ADC5 :ADC Input Channel 5; UART2RXD :Uart2 Data In(D);
22	PC4	I/O	GPIO	SPI1CLKB: SPI1 Clock(B); IIC_SCL_B：IIC Serial Clock(B); ALNK_DAT2B :Audio Link Data2(B); ADC4 : ADC Input Channel 4; UART2TXD: Uart2 Data Out(D); PWM4 :Timer4 PWM Output;
23	PC3	I/O	GPIO	LNA_EN ： External LNA enable; SPI0_DAT3A(3) : SPI0 Data3(A); SPI1DIB :SPI1 Data In(B); SFC_DAT3A(3) :SFC Data3(A); IIC_SDA_C : IIC Data(C); ALNK_LRCKB ： left and right channel frame clock; ADC3 :ADC Input Channel 3; UART0RXD :Uart0 Data In(D); TMR3 :Timer3 Clock In;

24	PC2	I/O	GPIO	PA_EN: External PA enable; PLNK_DAT1/ANCDE: Pdm Link Data1; SPI2DIB : SPI2 Data In(B); IIC_SCL_C：IIC Clock(C); ALNK_SCLKB : Audio Link Slave Clock(B); UART0TXD :Uart0 Data Out(D); TMR1: Timer1 Clock In;
25	USBDM	I/O	USB Negative Data (pull down)	SPI2DOB：SPI2 Data Out(B); IIC_SDA_A：IIC SDA(A); ADC11：ADC Input Channel 11; UART1RXD：UART1 Data In(D);
26	USBDP	I/O	USB Positive Data (pull down)	SPI2CLKB: SPI2 Clock(B); IIC_SCL_A：IIC Clock(A); ADC10 :ADC Input Channel 10; UART1TXD :Uart1 Data Out(D);
27	PA6	I/O	GPIO	UART1_RTS :Uart1 request to send; PLNK_DAT0/ANCDR :Pdm Link Data0; SPI2DOA : SPI2 Data Out(A); IIC_SDA_D : IIC Data(D); ALNK_DAT1AB ： Audio Link Data1(AB); ADC2 :ADC Input Channel 2; UART0RXA :Uart0 Data In(A); CAP0: Timer0 Capture;
28	PA5	I/O	GPIO	UART1_CTS :UART1 Clear to send; PLNK_SCLK/ANCCK:Pdm Link Slave Clock; SPI2CLKA: SPI2 Clock(A); IIC_SCL_D：IIC Clock(D); ALNK_DAT0AB ： Audio Link Data0(AB); ADC1: ADC Input Channel 1; UART0TXA :Uart0 Data Out(A); PWM5 :Timer5 PWM Output;
	PA3	I/O	GPIO	SPI1DOC :SPI1 Data Out(C); ALNK_DAT2A :Audio Link Data2(A); ADC0 :ADC Input Channel 0; UART2TXA :Uart2 Data Out(A); PWM1 :Timer1 PWM Output;
29	PA2	I/O	GPIO	CLKOUT1：Clock Out1; MICBIAS0 : MIC0 Bias Output(Built-in resistor); SPI1CLKC: SPI1 Clock(C); ALNK_MCLKA :Audio Link Main Clock(A); UART1RXC :Uart1 Data In(C); CAP3: Timer3 Capture;

30	PA1	I/O	GPIO	MICIN0 :MIC0 Input Channel 0; SPI1DIC: SPI1 Data In(C); UART1TXC :Uart1 Data Out(C); PWM0 :Timer0 PWM Output;
31	PA0	I/O	GPIO	MICLDO ： MIC0 Input Channel 0; SPI2DIA : SPI2 Data In(A); ALNK_DAT3A ： Audio Link Data3(A); UART2RXA :Uart2 Data In(A); CAP2: Timer2 Capture;
32	DACVSS	G		Ground;
BASE	VSS	G		Ground;

Pin Type	**Description**	**Pin Type**	**Description**
P	Power	I/O	Input or Output
PO	Power Output	I	Input
PI	Power Input	O	Output
G	Ground	RFI	Radio frequency interface
AO	Analog Output		

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
VPWR	Charger Voltage	-0.3	6	V
V_{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V_{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 PMU Characteristics

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.5	V	
VPWR	Charger supply Voltage	4.5	5.0	5.5	V	
Operating mode						
IOVDD	Voltage output	_	3.0	_	V	VBAT = 4.2V, 10mA loading
	Loading current	_	_	200	mA	IOVDD=3.2V@VBAT = 3.5V
DCVDD	Voltage output	_	1.25	_	V	IOVDD=3.0V, 10mA loading
	Loading current	_	_	60	mA	DCVDD=1.25V@IOVDD=3.0v on LDO mode
		_	_	150	mA	DCVDD=1.25V@VBAT=3.0v on DCDC mode
EVDD	Voltage output	_	1.1	_	V	DCVDD=1.25V, 1mA loading
	Loading current	_	_	5	mA	EVDD=1.1V@DCVDD=1.25v
Low Power mode						
IOVDD	Loading current	_	_	10	mA	IOVDD=3V@VBAT = 4.2V

3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charge Input Voltage	4.5	5	5.5	V	_
$V_{bat\ float}$	Charge Voltage	4.15	4.2	4.25	V	VPWR＞4.5V
I_{bat}	Charge Current	20	_	200	mA	Charge current at fast charge mode VBAT=4.0V@VPWR=5.0V
I_{end}	End Of Charge Current	2	_	30	mA	End of charge current
V_{Trikl}	Trickle Charge Voltage	_	3.0	_	V	VPWR＞4.5V

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{OL}	Low-Level Output Voltage	_	_	0.1* IOVDD	V	IOVDD = 3.0V
V_{OH}	High-Level Output Voltage	0.9* IOVDD	_	_	V	IOVDD = 3.0V

3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive(mA)		Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1~PA3,PA5,PA6 PB1~PB4,PB6,PB7 PC2~PC5	HD,HD0==0,0	2.4	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull Down 3、internal pull-up / pull-down resistance | accuracy ±20%
	HD,HD0==0,1	8			
	HD,HD0==1,0	26			
	HD,HD0==1,1	46			
PP0(VPWR) PB8	8 (High Voltage Resistant)		10K	10K	
PA0	8		10K	10K	
USBDP	4		1.5K	15K	
USBDM			180K	15K	

3.6 Audio DAC Characteristics

Audio Format: SBC Table 3-6

Parameter	MODE	Min	Typ	Max	Unit	Test Conditions
Frequency Response		20	_	20k	Hz	1KHz/0dB 32 ohm loading With A-Weighted Filter
Output Swing	Differential	_	0.35	1.18	Vrms	
	Single-ended	_	0.35	0.67	Vrms	
THD+N	Differential	_	-69	_	dB	
	Single-ended	_	-68	_	dB	
S/N	Differential	_	95	101	dB	
	Single-ended	_	95	98	dB	
Dynamic Range	Differential	_	96	102	dB	1KHz/-60dB 32 ohm loading With A-Weighted Filter
	Single-ended	_	96	98	dB	
Noise Floor	Differential	_	5.8	_	uVrms	A-Weighted Filter
	Single-ended	_	6	_	uVrms	
DAC Output Power	Differential	_	3.9	43	mW	32ohm loading
	Single-ended	_	3.9	14	mW	

3.7 Audio ADC Characteristics

Audio Filter: A-Weighted Table 3-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	_	90	_	dB	Fsample=44.1kHz,Gain=6dB Fin=1KHz 320mVrms
SNR	_	90	_	dB	Fsample=44.1kHz,Gain=6dB Fin=1KHz 320mVrms
THD+N	_	-70	_	dB	
SNR	_	85	_	dB	Fsample=44.1kHz,Gain=16dB Fin=1KHz 90mVrms
THD+N	_	-65	_	dB	

3.8 BT Characteristics

3.8.1 Transmitter

Basic Data Rate **Table 3-8**

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power，DH5			6		dBm	25℃， Power Supply VBAT=3.7V 2441MHz 4 Layer Board
RF Power Control Range，DH1			20		dB	
20dB Bandwidth，DH5			920		KHz	
Adjacent Channel Transmit Power，DH1（BQB Test Mode RF_Tx Power=3.6dBm）	+2MHz		-51		dBm	
	-2MHz		-46		dBm	
	+3MHz		-51		dBm	
	-3MHz		-43		dBm	

Enhanced Data Rate **Table 3-9**

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-1.4		dB	25℃ Power Supply VBAT=3.7V 2441MHz 2DH5 4 Layer Board
π/4 DQPSK Modulation Accuracy	DEVM RMS		6		%	
	DEVM 99%		10		%	
	DEVM Peak		13		%	
In-band spurious Emissions（BQB Test Mode RF_Tx Power=3.6dBm）	+2MHz		-41		dBm	
	-2MHz		-36		dBm	
	+3MHz		-44		dBm	
	-3MHz		-36		dBm	

3.8.2 Receiver

Basic Rate **Table 3-10**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-91		dBm	25℃， Power Supply VBAT=3.7V 2441MHz DH1 4 Layer Board
Co-channel Interference Rejection			4		dB	
Adjacent Channel Interference Rejection	+1MHz		-27		dB	
	-1MHz		-25		dB	
	+2MHz		-41		dB	
	-2MHz		-37		dB	
	+3MHz		-45		dB	
	-3MHz		-33		dB	

Enhanced Data Rate **Table 3-11**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	25℃, Power Supply VBAT=3.7V 2441MHz 2DH5 4 Layer Board
Co-channel Interference Rejection			10		dB	
Adjacent Channel Interference Rejection	+1MHz		-27		dB	
	-1MHz		-26		dB	
	+2MHz		-30		dB	
	-2MHz		-28		dB	
	+3MHz		-37		dB	
	-3MHz		-26		dB	

3.9 ESD Protection

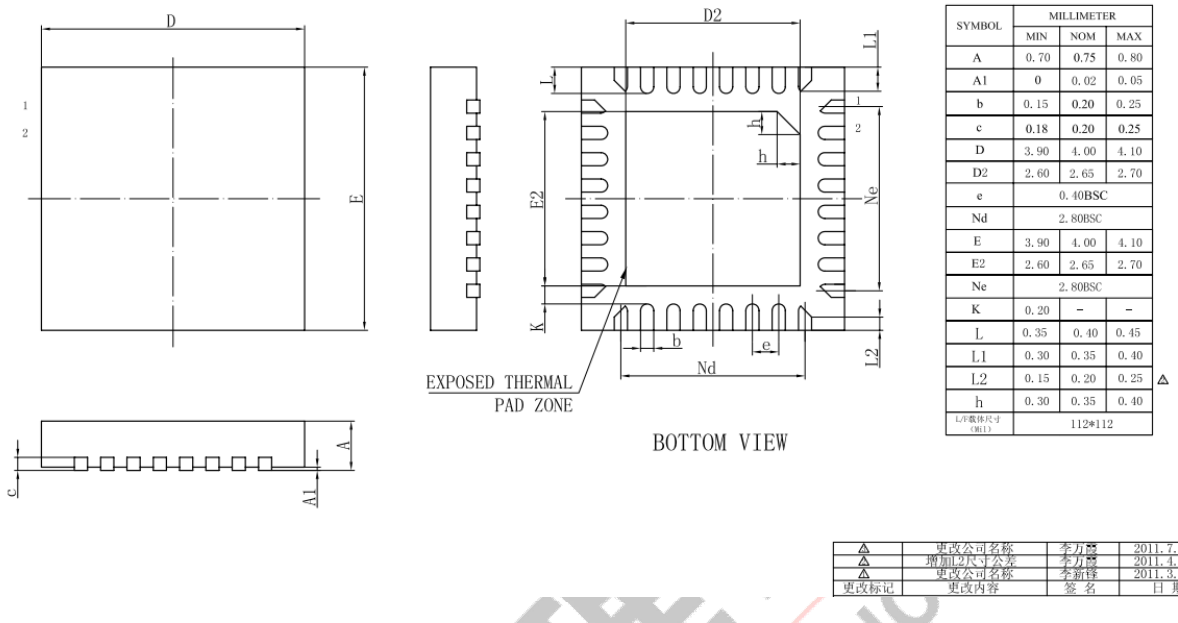
Table 3-12

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

4 Package Information

4.1 QFN32_4.0x4.0



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25 △
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	112*112		

△	更改公司名称	李力	2011.7.5
△	增加L2尺寸公差	李力	2011.4.18
△	更改公司名称	李新锋	2011.3.3
更改标记	更改内容	签 名	日 期

Figure 4-1 AC7026A Package

5 Solder-Reflow Condition

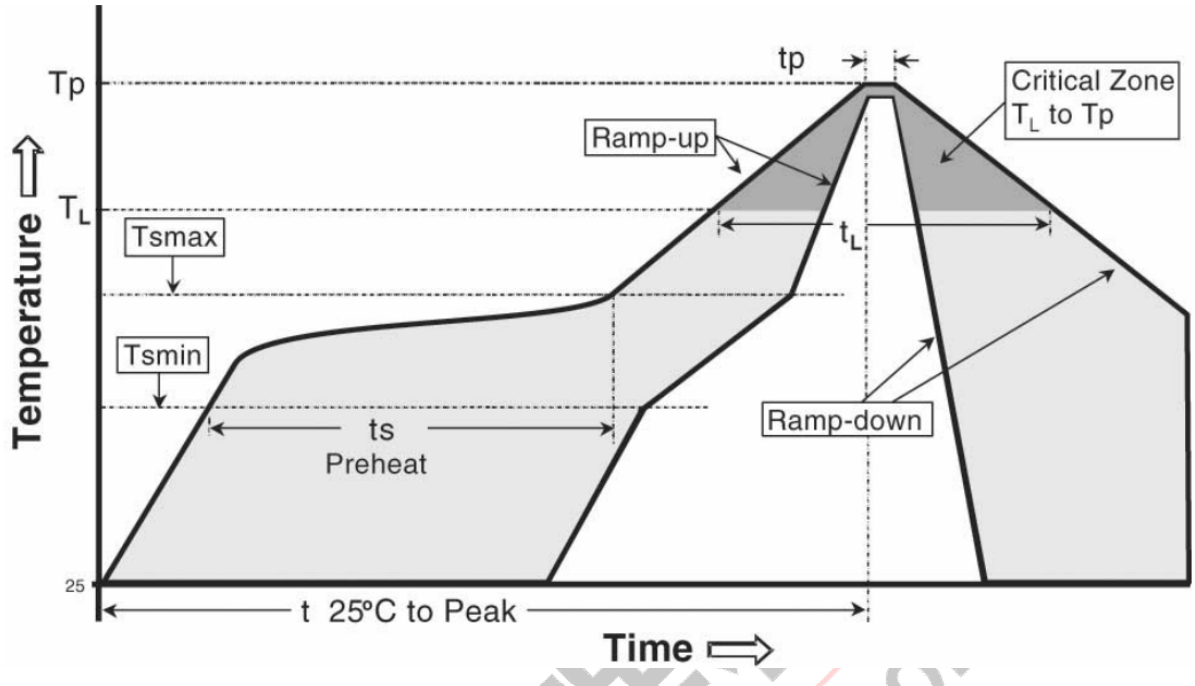


Figure 5-1 Classification Reflow Profile

Classification Profiles **Table 5-1**

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100℃	150℃
	Temperature Max (T_{smax})	150℃	200℃
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183℃ 60-150 seconds	217℃ 60-150 seconds
Peak package body temperature (T_p)		See Table 5-2	See Table 5-3
Time within 5℃ of actual Peak Temperature (tp)[2]		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6℃/second max	6℃/second max
Time 25℃ to peak temperature		6 minutes max	8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a "supplier" minimum and "user" maximum.

SnPb - Classification Temperature **Table 5-2**

Package Thickness	Volume mm^3 < 350	Volume mm^3 ⩾ 350
<2.5 mm	240 +0/-5℃	225 +0/-5℃
⩾2.5 mm	225 +0/-5℃	225 +0/-5℃

Pb-free - Classification Temperature **Table 5-3**

Package Thickness	Volume mm³ < 350	Volume mm³ 350 - 2000	Volume mm³ > 2000
< 1.6mm	260℃	260℃	260℃
1.6 mm - 2.5mm	260℃	250℃	245℃
> 2.5mm	250℃	245℃	245℃

*Tolerance:The device manufancturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C.For example 260°C+0°C)at the rated MSL level.

6 Revision History

Date	Revision	Description
2022.09.06	V1.0	Initial Release

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