AC7003F4 Datasheet

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AC7003F4 Features

CPU

- 32bit Dual-Issue DSP
- Up to 160MHz programmable processor
- With IEEE754 Single precision FPU
- With cordic accelerate engine
- Advanced debug with 8 hardware breakpoints/watchpoints
- Advanced system execption capture unit

Interrupt

- Support for up to 64 interrupts with 8 priority level
- NMI supported
- SWI supported, with configurable priority
- Low power wake up by polling pending 7 IO interrupts for low power wake up

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 20-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC, SNR >= 102dB
- One channels 24-bit ADC , SNR >= 95dB
- DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/ 32kHz/44.1kHz/48kHz/64kHz/88.2kHz/ 96kHz are supported
- ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/ 32kHz/44.1kHz/48kHz are supported
- Two analog MIC amplifier, build-in MIC bias generator
- Supports Four PDM digital MIC inputs
- Two channels analog AUX , supports Stereo
- Supports cap-less, single-ended, and Two differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V5.3+BR+EDR+BLE specification
- Meet class2 and class3 transmitting power requirement
- Support GFSK and DQPSK all packet types
- Provides maximum +10dbm transmitting power
- EDR receiver with minimum -94dBm sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\ gatt\rfcomm\sdp\l2cap profile
- a2dp 1.3.2\avctp 1.4\avdtp 1.3\ avrcp 1.6.2\ hfp 1.8 \spp 1.2\rfcomm 1.1\pnp 1.3\ hid 1.1.1\sdp core5.3\l2cap core 5.3

Peripherals

- One full speed USB 2.0 OTG controller
- Six multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex basic UART, UART0、UART1 support DMA mode
- One hardware IIC interface supports host and device mode
- LED controller，support 2LED control by one IO
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs
- Crossbar IO support: timer\SPI\SDC\IIC \UART\RDEC\ALINK\PLINK

PMU

- Low voltage LDO and DC-DC for internal digital and analog circuit supply
- Less 2uA current consumption in the soft-off mode
- Built-in LDO and DC-DC for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 4.4V
- IOVDD is 2.2V to 3.6V

Packages

- QFN20(3mm*3mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Bluetooth Stereo Headsets and Headphones

1、Pin Definition

1.1 Pin Assignment

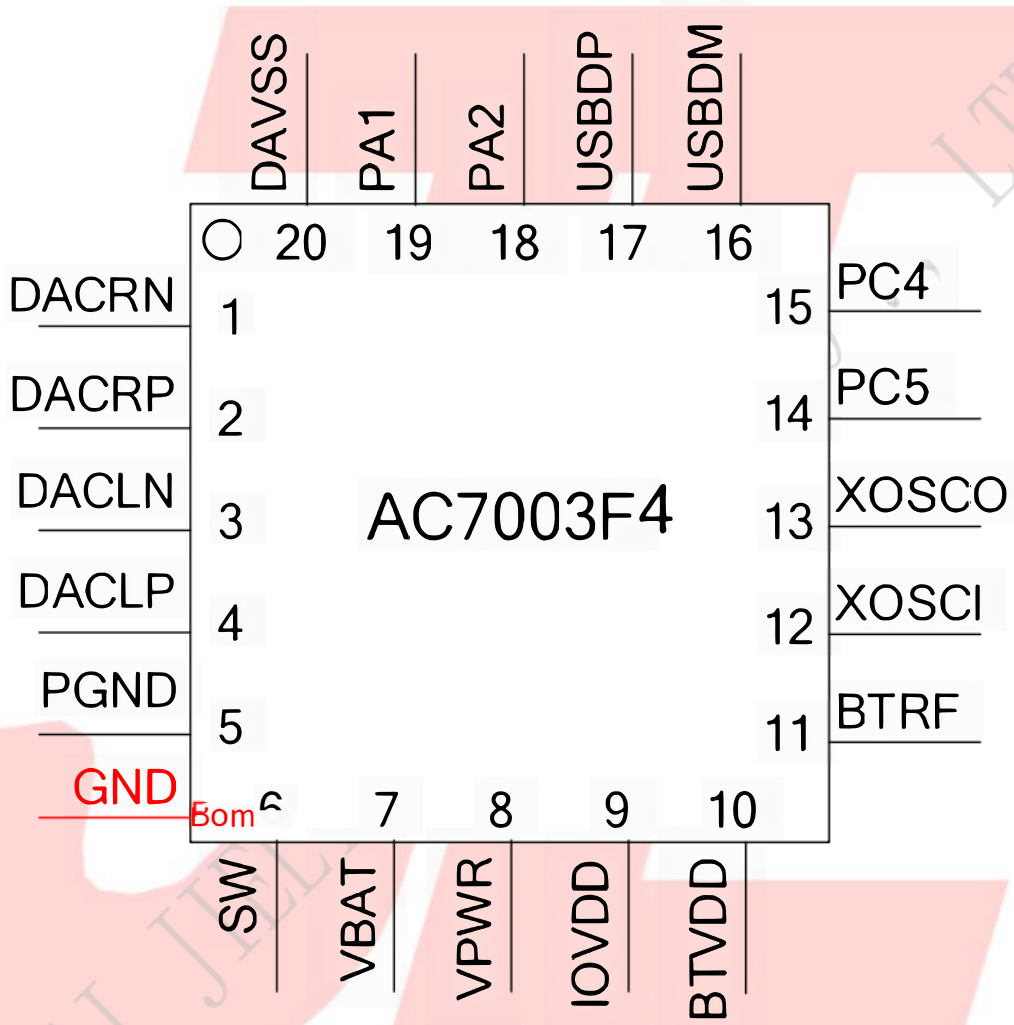


Figure 1-1 AC7003F Package Diagram

1.2 Pin Description

Table 1-1 AC7003F Pin Description

PIN NO.	Name	I/O Type	Drive (mA) 4 level	Function	Other Function
1	DACRN	O	/		Different DAC Right Negative Channel
2	DACRP	O	/		Different DAC Right Positive Channel
3	DACLN	O	/		Different DAC Left Negative Channel
4	DACLP	O	/		Different DAC Left Positive Channel
5	PGND	P	/		DCDC Ground
6	SW	P	/		DCDC switch output, connected to inductor
7	VBAT	PI	/		Power Supply, connect to battery
8	VPWR	PI	/		Charge Power Input;
		I/O	8	GPIO	High Voltage Resistance I/O; UART0TXC：Uart0 Data Output(C); UART0RXC：Uart0 Data Input(C); PWM3：Timer3 PWM Output； CAP1：Timer1 Capture;
9	IOVDD	PO	/		IO Power 3.3v
10	BTVDD	PO	/	GPIO	BT Power
11	BTRF	/	/		BT Antenna
12	XOSCI	I	/		XOSC In
13	XOSCO	O	/		XOSC Out
14	PC5	I/O	2.4~64	GPIO	SD0CLKA: SD0 Clock(A); UART2RXD：Uart2 Data Input(D); SPI1DOB：SPI1 Data Out(B); ALNK_DAT3(B)：Audio Link Data3(B); IIC_SDA_B：IIC SDA(B)； ADC5：ADC Input Channel 5；
15	PC4	I/O	2.4~64	GPIO	SD0CMDA: SD0 CMD(A); UART2TXD：Uart2 Data Output(D); SPI1CLKB：SPI1 Clock(B); ALNK_DAT2(B)：Audio Link Data2(B); IIC_SCL_B：IIC SCL(B)； ADC4：ADC Input Channel 4； PWM4：Timer4 PWM Output；
16	USBDM	I/O	4	USB Negative Data	UART1RXD：Uart1 Data Input(D)； IIC_SDA_A：IIC SDA(A)； ADC11：ADC Input Channel 11；

					SPI2DOB: SPI2 Data Out(B); ISP_DI:
17	USBDP	I/O	4	USB Positive Data	UART1TXD：Uart1 Data Output(D)； IIC_SCL_A：IIC SCL(A)； ADC10：ADC Input Channel 10； SPI2CLKB: SPI2 Clock(B); ISP_CLK:
18	PA2	I/O	2.4~64	GPIO	ALNK_MCLK(A)：ALNK Master Clock(A); MIC_BIAS0：MIC0 Bias Output； MIC0_N：Different MIC0 Negative AMUX_A1：Analog Channel A1 L/R Input; CAP3：Timer3 Capture； UART1RXC：Uart1 Data In(C)； CLKOUT1:
19	PA1	I/O	2.4~64	GPIO	MIC0：MIC0 Input Channel ; MIC0_P：Different MIC0 Positive AMUX_A0：Analog Channel A0 L/R Input; PWM0：Timer0 PWM Output； UART1TXC：Uart1 Data Output(C)；
20	DAVSS	P	/		Analog Ground
/	Bom	P	/		Ground

P: Power or Ground PO:Power Output PI:Power Input I/O:Input or Output I:Input O:Output

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
VPWR	Charger Voltage	-0.3	6	V
$V_{3.0IO}$	3.0V IO Input Voltage (IOVDD)	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.4	V	
VPWR	Charger supply Voltage	4.5	5.0	5.5	V	
Normal mode						
IOVDD	Voltage output	_	3.0	_	V	VBAT = 4.2V, 10mA loading
	Loading current	_	_	100	mA	IOVDD=3.0V@VBAT = 4.2V
BTVDD	Voltage output	_	1.25	_	V	IOVDD=3.0V, 10mA loading
	Loading current	_	_	60	mA	BTVDD=1.25V@IOVDD=3.0v
EVDD	Voltage output	_	1.1	_	V	BTVDD=1.25V, 1mA loading
	Loading current	_	_	5	mA	EVDD=1.1V@BTVDD=1.25v
LP mode						
IOVDD	Loading current			5	mA	IOVDD=3V@VBAT = 4.2V

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charge Input Voltage	4.5	5	5.5	V	_

V_{Charge}	Charge Voltage	4.15	4.2	4.25	V	VPWR＞4.5V
		4.30	4.35	4.40	V	VPWR＞4.65V
I_{Charge}	Charge Current	20		200	mA	Charge current at fast charge mode
I_{Trikl}	Trickle Charge Current	20	45	70	mA	$V_{BAT}<V_{Trikl}$

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	–	IOVDD+0.3	V	IOVDD= 3.0V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	–	–	0.33	V	IOVDD= 3.0V
V_{OH}	High-Level Output Voltage	2.7	–	–	V	IOVDD = 3.0V

2.5 Internal Resistor Characteristics

Table 2-5

Port	**Drive(mA)**				**Internal Pull-Up Resistor**	**Internal Pull-Down Resistor**	**Comment**
PA0~PA8 PC4、PC5	2.4	8	26.4	64	10K	10K	1、USBDM & USBDP default pull Down 2、PP0(VPWR) are high voltage resistance to 5V 3、internal pull-up/pull-down resistance | accuracy ±20%
PP0(VPWR)	8				10K	10K	
USBDP	4				1.5K	15K	
USBDM	4				180K	15K	

2.6 DAC Characteristics

Table 2-6

Parameter	**Min**	**Typ**	**Max**	**Unit**	**Audio Format**	**Test Conditions**

Frequency Response	20	_	20K	Hz	_	Differential Mode 1KHz/0dB 32 ohm loading With A-Weighted Filter
Output Swing		0.56	0.72	Vrms	_	
THD+N	_	-78	_	dB	PCM	
	_	-69.6	_	dB	SBC	
S/N	_	100	102	dB	PCM	
	_	99.4	_	dB	SBC	
Crosstalk	_	-113	_	dB	_	
Dynamic Range	_	100.2	_	dB	PCM	Differential Mode 1KHz/-60dB 32 ohm loading With A-Weighted Filter
	_	99.9	_	dB	SBC	
Noise Floor		6.0		uV	_	A-Weighted Filter
DAC Output Power	_	9.7	16.0	mW	_	Differential Mode 32ohm loading

2.7 ADC Characteristics

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		95		dB	Fsample=44.1kHz Fin=1KHz 2mVpp Input
S/N	_	95	_	dB	Fsample=44.1kHz Fin=1KHz 2Vpp Input
THD+N	_	-72	_	dB	
Crosstalk	_	-80	_	dB	

2.8 BT Characteristics

2.8.1 Transmitter

Basic Data Rate **Table 2-8**

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power			7.9	10	dBm	25℃, Power Supply VBAT=3.7V 2441MHz 2 Layer Board
RF Power Control Range			18.3		dB	
20dB Bandwidth			950		KHz	
Adjacent Channel Transmit Power	+2MHz		-40		dBm	
	-2MHz		-38		dBm	
	+3MHz		-44		dBm	
	-3MHz		-35		dBm	

Enhanced Data Rate **Table 2-9**

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-1.2		dB	25℃, Power Supply VBAT=3.7V 2441MHz 2 Layer Board
π/4 DQPSK Modulation Accuracy	DEVM RMS	6	9.7		%	
	DEVM 99%	10	22.1		%	
	DEVM Peak	15	17.2		%	
Adjacent Channel Transmit Power	+2MHz		-40		dBm	
	-2MHz		-38		dBm	
	+3MHz		-44		dBm	
	-3MHz		-35		dBm	

2.8.2 Receiver

Basic Data Rate **Table 2-10**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-91		dBm	25℃, Power Supply VBAT=3.7V 2441MHz DH5 2 Layer Board
Co-channel Interference Rejection			-10		dB	
Adjacent Channel Interference Rejection	+1MHz		+4		dB	
	-1MHz		+2		dB	
	+2MHz		+38		dB	
	-2MHz		+38		dB	
	+3MHz		>+40		dB	
	-3MHz		+34		dB	

Enhanced Data Rate **Table 2-11**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25℃, Power Supply VBAT=3.7V 2441MHz 2DH5 2 Layer Board
Co-channel Interference Rejection			-11		dB	
Adjacent Channel Interference Rejection	+1MHz		+4		dB	
	-1MHz		+2		dB	
	+2MHz		+38		dB	
	-2MHz		+38		dB	
	+3MHz		>+40		dB	
	-3MHz		+34		dB	

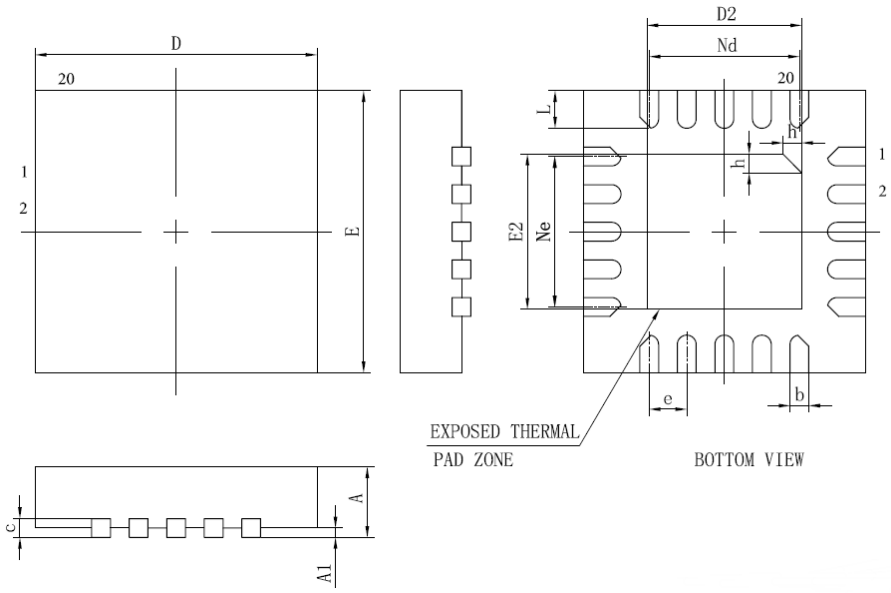
2.9 ESD Protection

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage

3、 Package Information

3.1 QFN20_3.0x3.0



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸 (MIL)	75*75		

Figure 3-1 AC7003F Package

4、Revision History

Date	Revision	Description
2021.05.13	V1.0	Initial Release
2021.05.27	V1.1	Update Electrical Characteristics
2021.08.03	V1.2	Update Bluetooth and profile Visions
2021.08.24	V1.3	Update Audio and Bluetooth Characteristics
2021.12.29	V1.4	Add Chip ESD Protection Characteristics