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XINBOLE

Product Specification

XBLW UC3844

Current Mode Pulse-width Controller

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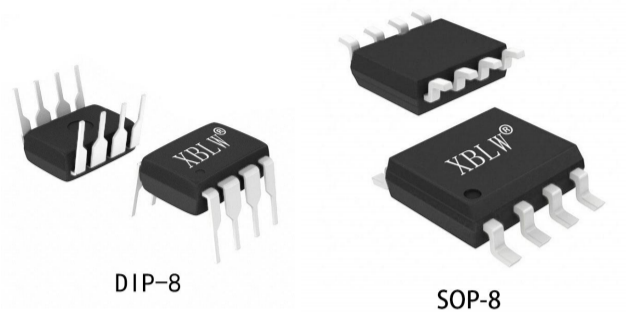
Descriptions

The UC3844 is a pulse width integrated circuit with current control mode for switching power supply. Compared with the voltage control mode, it has many advantages in load response and linear adjustment.
This device is available in SOP8 package and DIP8 package.



Feature

- Internally Undervoltage Lockout Circuit
- Low Startup and Operating Current（0.26mA at typical）
- Maximum Duty Cycle Control
- High current push-pull output (drive current up to 1A)
- Operating Frequency: 500kHz
- Automatic Feed Forward Compensation
- Double-pulse Suppression
- Enhanced Load-response Characteristics

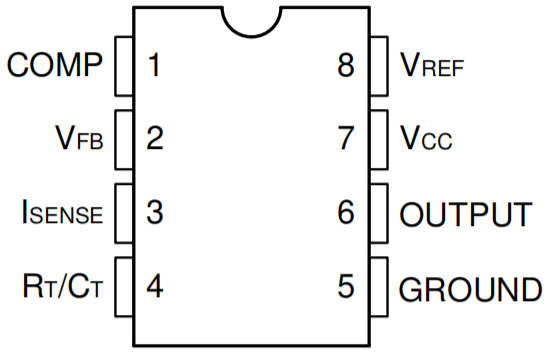
Applications

- Switching regulators of any polarity
- Transformer-coupled DC-DC converters

Ordering Information

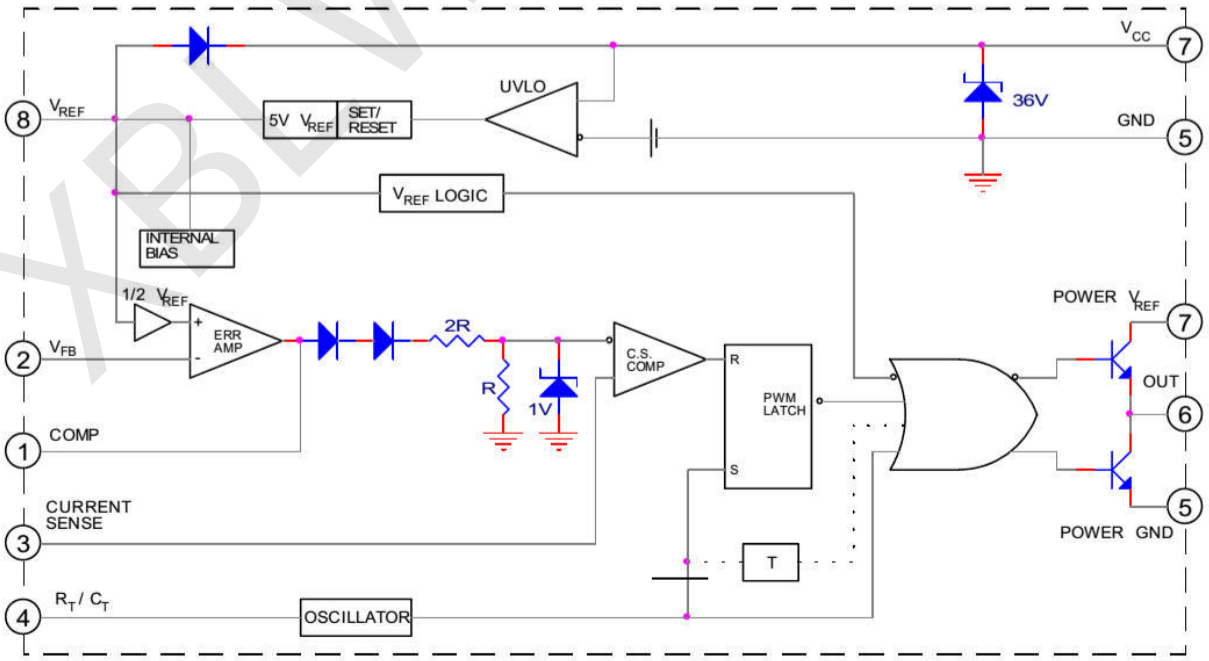
Product Model	Package Type	Marking	Packing	Packing Qty
XBLW UC3844AN	DIP-8	UC3844AN	Tube	2000pcs/Box
XBLW UC3844BDTR	SOP-8	UC3844B	Tape	2500pcs/Reel

Pins Description



No.	Symbol	Function	No.	Symbol	Function
1	COMP	Compensation	5	GND	Ground
2	V_{FB}	Voltage Feedback	6	OUTPUT	Output
3	I SENSE	Input Current Sense	7	V_{CC}	Power Supply
4	R_T / C_T	Oscillator	8	V_{REF}	Reference Voltage

Function Diagram



Maximum Ratings

Tamb =2 5 ℃ ,unless otherwise noted

Rating	Symbol	Value	Unit
Power voltage	V_{CC}	30	V
Output Current	I_O	± 1	A
Error Amp Sink Current	Isink （EA）	10	mA
Error Amp. Input Voltage	Vin （EA）	-0.3~+6.3	V
Power Dissipation	PD(DIP)	1	W
Operating Ambient Temperature	T_{amb}	0 ~ 70	℃
Storage Temperature Range	T_{stg}	-55 ~ 150	℃

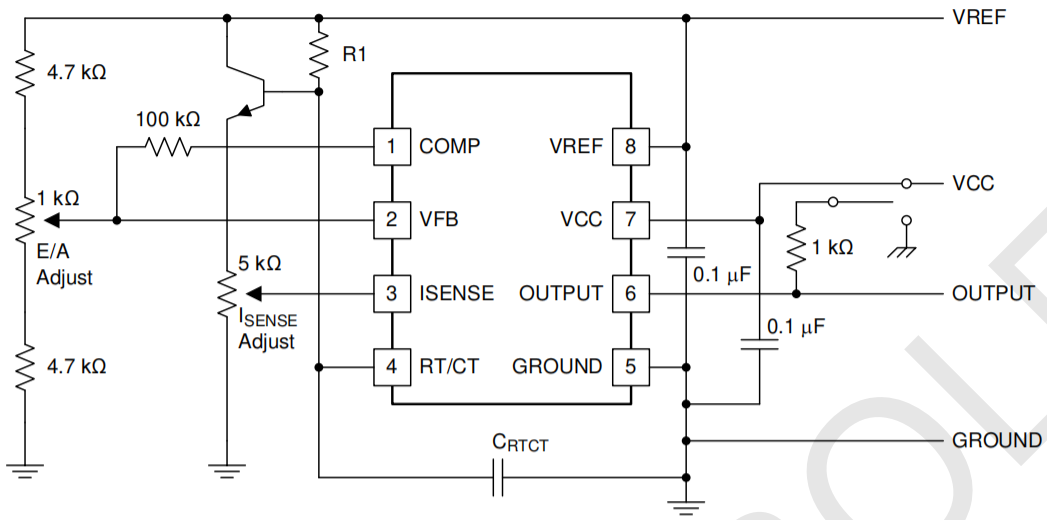
Electrical Characteristics

（V_{CC}= 15 V ， Ta= 0 ~ 70 ℃ ， R_T = 10KΩ ， C_T = 3 . 3nF, unless otherwise noted ）

Characteristic	Test conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Reference Section						
Reference Output Voltage	Tj=25℃ I_{REF}= 1mA	Vref	4.9	5	5.1	V
Line Regulation rate	12V ≤V_{CC}≤25 V	ΔVref		6	20	mV
Load Regulation	1mA ≤I_{REF}≤20 mA	ΔVref		6	25	mV
Output Short Circuit Current	Tamb=25 ℃	Isc	-30	-80	-180	mA
Oscillator Section						
Frequency	Ta= 25 ℃	fosc	47	52	57	kHz
Frequency Change with Voltage	12V ≤V_{CC}≤25 V	Δf/Δ V_{CC}		0.05	1	%
Oscillator Voltage Swing	peak to peak	$V_{(OSC)}$		1.6		Vpp

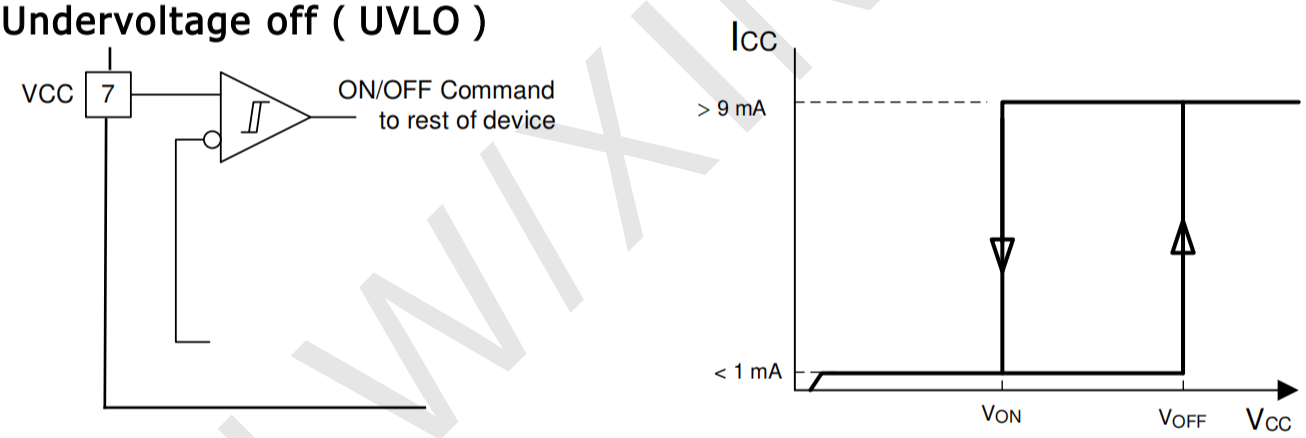
Error Amplifier Section						
Input Bias Current		I_{BIAS}		-0.1	-2	μA
Input voltage	V_1=2.5V	$V_{in\ (EA)}$	2.42	2.5	2.58	V
Open Loop Voltage Gain	2V ≤Vo≤4V	G_{VO}	60	90		dB
Power Supply Rejection Ratio	12V ≤V_{CC}≤25 V	PSRR	60	70		dB
Output Current – Sink	V_2=2.7V， V_1=1.1V	I_{SINK}	2	6.5		mA
Output Current –Source	V_2=2.3V， V_1=5V	I_{SOURCE}	-0.5	-0.9		mA
Output Voltage Swing (High State)	V_2=2.3V， R_L=15kΩ to GND	V_{OH}	5	6.4		V
Output Voltage Swing (Low State)	V_2=2.7V， R_L=15kΩ to Pin 8	V_{OL}		0.87	1.1	V
Current Sense Section						
Current Sense Input Voltage Gain		G_V	2.85	3	3.15	V/V
Maximum Current Sense Input Threshold	V1=5V	$V_{I\ (MAX)}$	0.9	1	1.1	V
Power Supply Rejection Ratio	12V ≤V_{CC}≤25 V	PSRR		70		dB
Input Bias Current		I_{BIAS}		-2	-10	μA
Output Section						
Output Voltage Low State	Isink=20mA	V_{OL}		0.1	0.4	V
	Isink=200mA			1.5	2.2	V
Output Voltage High State	Isource=20mA	V_{OH}	13	13.5		V
	Isource=200mA		12	13		V
Output Voltage Rise Time	Cl=1nF	tr		50	150	ns
Output Voltage Fall Time	Cl=1nF	tf		50	150	ns
Undervoltage Lockout Section						
Startup Threshold		$V_{TH(ST)}$	14.5	15.5	17.5	V
Minimum Operating Voltage After Turn-On		$V_{OPR(MIN)}$	8.5	9.8	11.5	V
PWM Section						
Duty Cycle Maximum		Dmax	45	48	50	%
Duty Cycle Minimum		Dmin			0	%
Total Device						
Power Supply Current (Startup)		I_{ST}		0.26	0.5	mA
Power Supply Current(Operating)	V_3=V_2=0V	$I_{CC(OPR)}$		11	17	mA
Power Supply Zener Voltage	Icc=25mA	V_Z		34		V

Basic Test Circuit Diagram



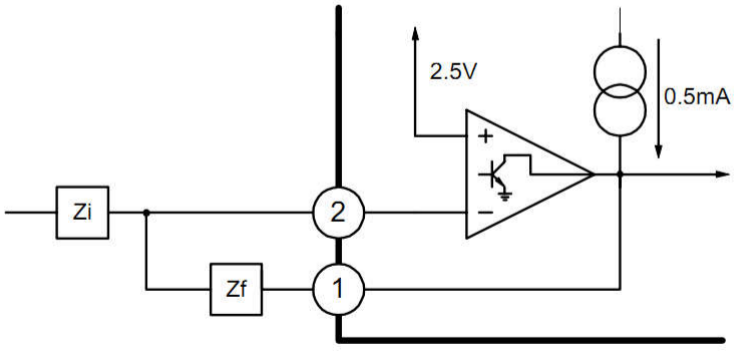
Grounding techniques should be carefully considered when there are high peak currents associated with capacitive loads. The timing and bypass capacitors must be installed next to the PIN5 and single-point grounded. Transistors and 5kΩ potentiometers are used to sample waveforms and send waveforms with adjustable slopes to PIN3.

Undervoltage off (UVLO)



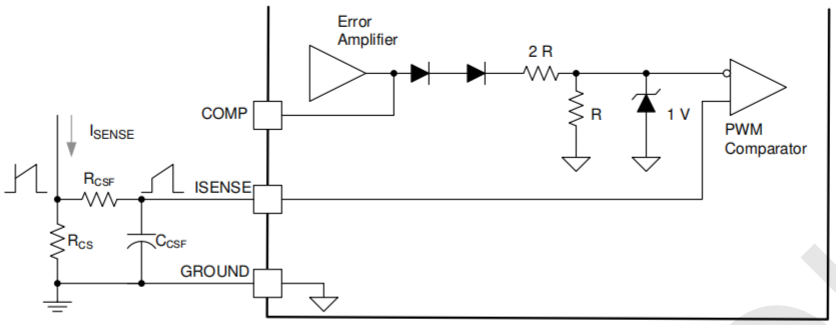
The output driver is placed in a high impedance state when entering an undervoltage shutdown. The sixth pin must be grounded with a leakage resistance to prevent leakage current from pushing the power switch

Error amplifier connection



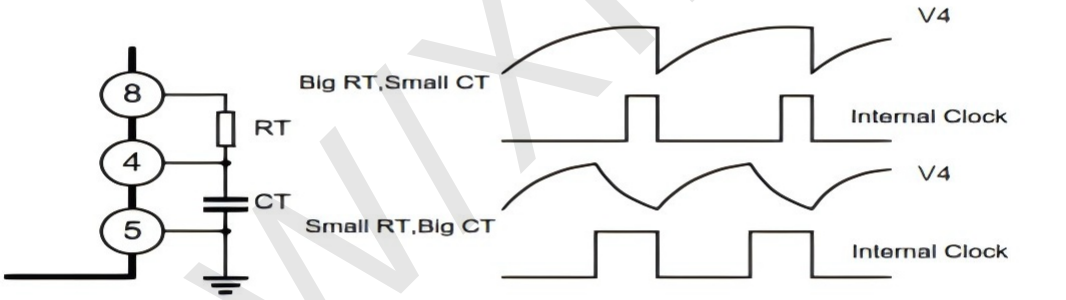
Error amplifier can push-pull output 0.5 ma current

Current detection circuit



Peak current (IS) IS defined as: $I_{S(MAX)} \approx 1.0\ V/R_S$ requires a small RC filter network to suppress the transient response of the switch.

Oscillator waveform and maximum duty cycle, period



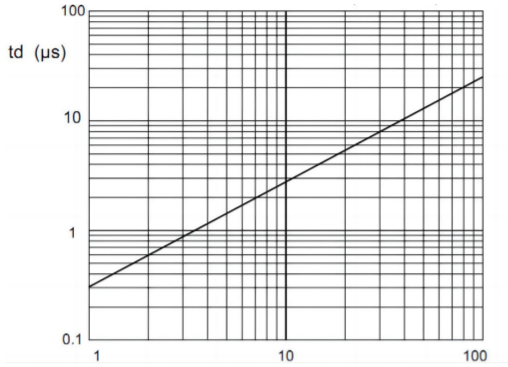
The oscillating time capacitor CT is charged by VREF via RT and discharged by an internal current source. The internal clock signal drives the output to a low level during discharge. The oscillation period and the maximum duty cycle can be determined by selecting RT and CT simultaneously. The time of charge and discharge is determined by the following formula:

$$t_c \approx 0.55 R_T * C_T$$

$$t_d \approx R_T * C_T * \ln\left(\frac{0.063R_T - 2.7}{0.063R_T - 4}\right)$$

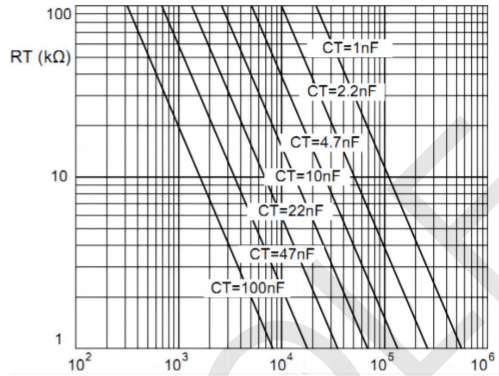
The frequency is: $f=(tc+td)^{-1}$

When: $R_T > 5K\Omega$, $f \approx \frac{1.8}{R_T * C_T}$



Electrical time capacitance (nF)

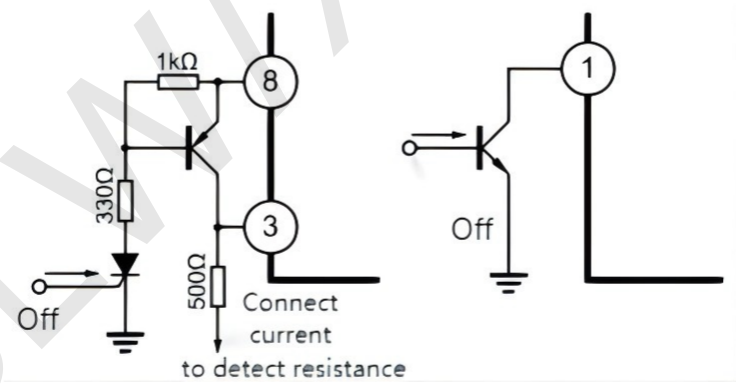
Relationship between oscillation dead time and capacitance CT



Frequency (Hz)

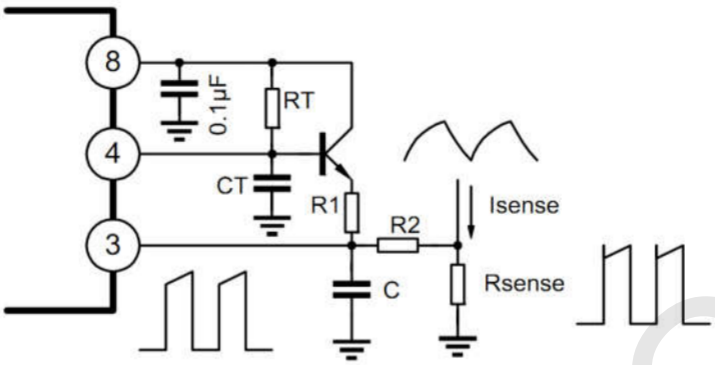
Relationship between frequency and timing resistance

Off technology

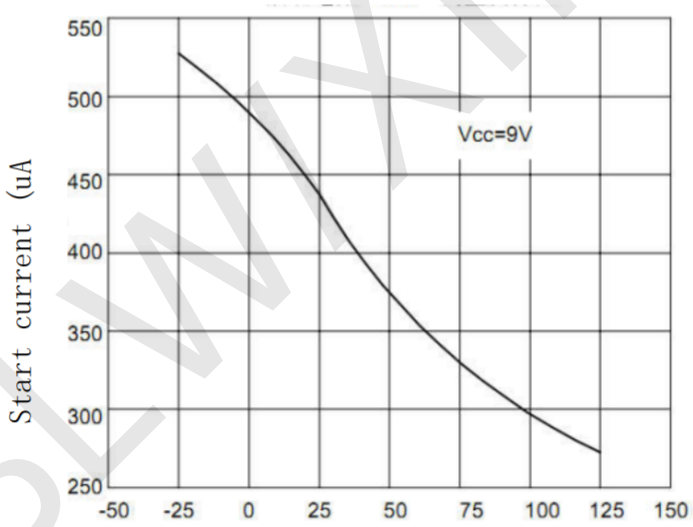


The shutdown of UC3844 can be accomplished in two ways: by raising the No. 3 pin voltage above 1V or by lowering the No. 1 pin voltage to within the forward voltage drop of the two diodes at the ground level, both methods make the output of the PWM comparator high (see internal block diagram) . The PWM latch trigger is preferentially reset so that the output is kept at a low level until the next clock cycle after the off signal of Pin 1 or Pin 3 is removed. An example of an external latch-off is achieved by adding a one-way SCR, which resets when the supply voltage VCC is below the UVLO threshold. At this point, the SCR is allowed to reset when the reference voltage is turned off.

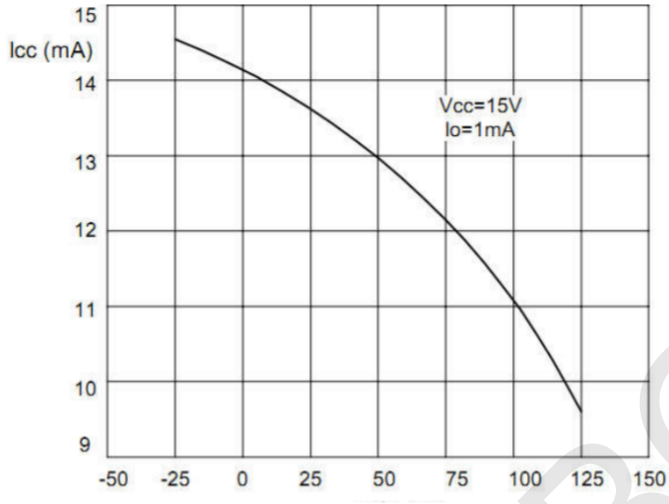
Slope Compensation



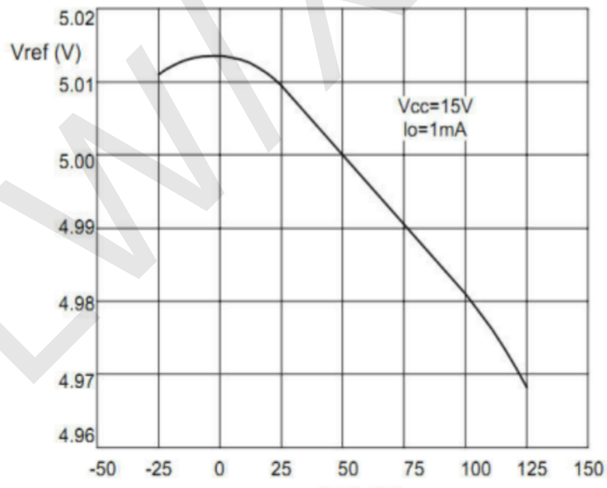
A fraction of the oscillator ramp can be summed resistively with the current-sense signal to provide slope compensation for converters requiring duty cycles over 50% . Note that capacitor CCSF forms a filter with RCSF to suppress the leading-edge switch spikes.



Start current IST temperature characteristics



Temperature characteristics of power dissipation current ICC

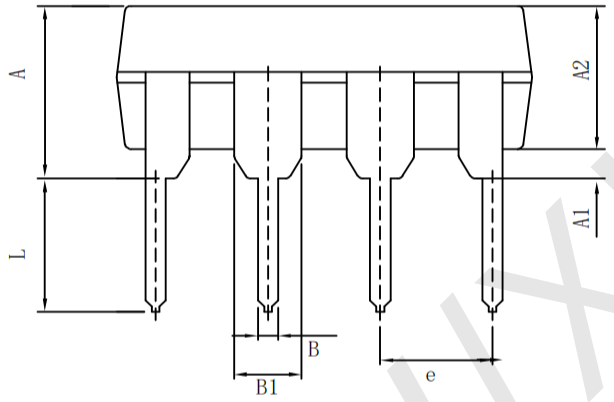


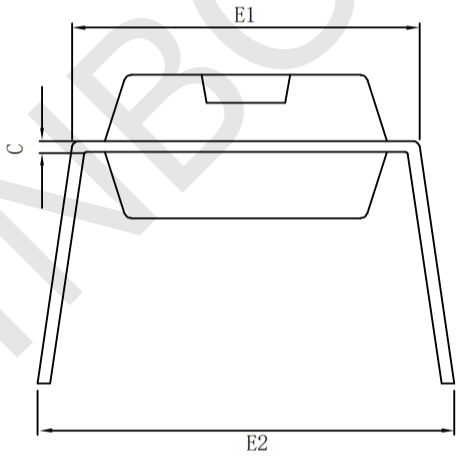
Refer to the temperature characteristics of the voltage source Vref

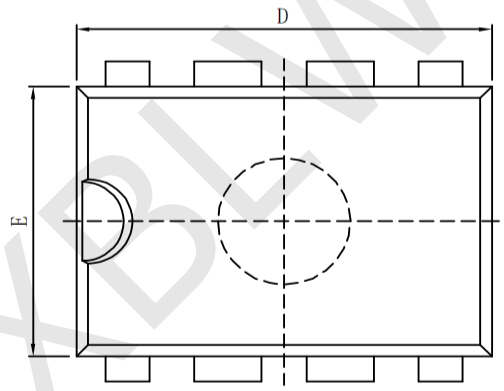
Package Information

- DIP-8

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	9.000	9.400	D	0.354	0.370
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354

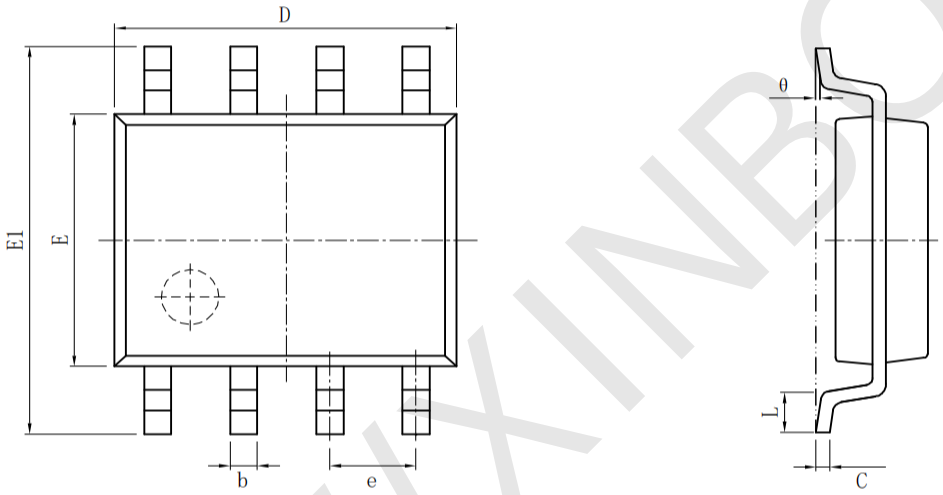


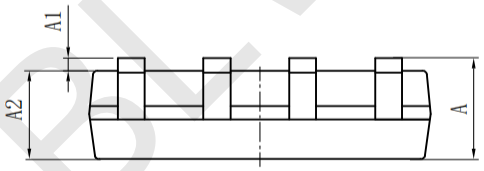




- SOP-8

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.053	0.069
A1	0.100	0.250	A1	0.004	0.010
A2	1.350	1.550	A2	0.053	0.061
b	0.330	0.510	b	0.013	0.020
c	0.170	0.250	c	0.006	0.010
D	4.700	5.100	D	0.185	0.200
E	3.800	4.000	E	0.150	0.157
E1	5.800	6.200	E1	0.228	0.224
e	1.270(BSC)		e	0.050(BSC)	
L	0.400	1.270	L	0.016	0.050
θ	0°	8°	θ	0°	8°





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