3-Phase Brushless DC Motor Pre-Driver

Chip Description

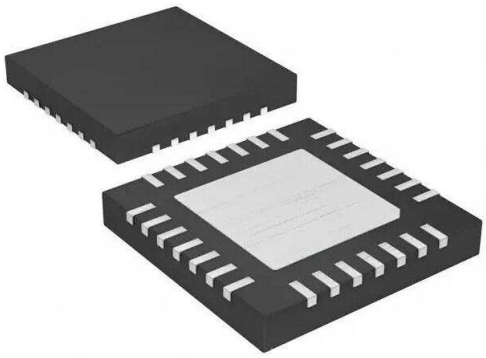
GC4931P is a complete 3-phase brushless DC motor pre-driver. The device is capable of driving a wide range of N-channel power MOSFETs and can support motor supply voltages up to 36 V. Commutation logic is determined by three Hall-element inputs spaced at 120°.

Other features include fixed off-time pulse width modulation (PWM) current control for limiting inrush current, locked-rotor protection with adjustable delay, thermal shutdown, over voltage monitor, and synchronous rectification. Internal synchronous rectification reduces power dissipation by turning on the appropriate MOSFETs during current decay, thus shorting the body diode with the low RDS(on) MOSFET. Over voltage protection disables synchronous rectification when the motor pumps the supply voltage beyond the over voltage threshold during current recirculation.

The GC4931P offers enable, direction, and brake inputs that can control current using either phase or enable chopping. Logic outputs FG1, FG2 can be used to accurately measure motor rotation. Output signals toggle state during Hall transitions, providing an accurate speed output to a microcontroller or speed control circuit.

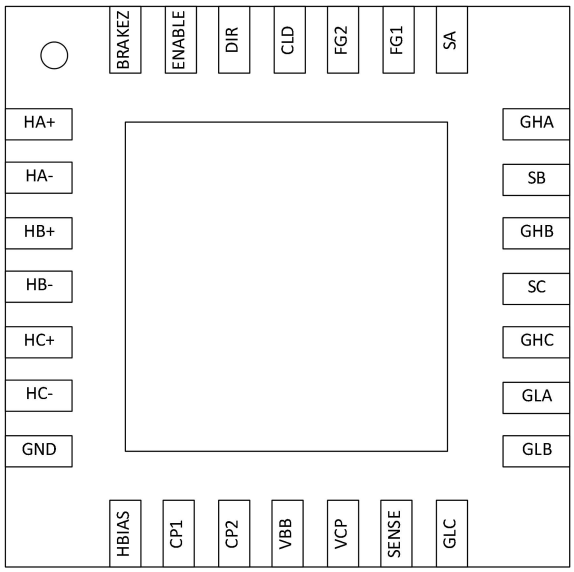
Chip Features

- Drives 6 N-channel NMOSFETs
- Wide operating voltage 4.7~36V
- Synchronous rectification for low power dissipation
- Hall element inputs
- Internal UVLO and thermal shutdown circuitry
- Standby mode
- FG outputs
- Dead time protection
- Lock detect protection
- Over voltage protection



Part Number	Package Type	Body Size
GC4931P	QFN28	5*5*0.8, e=0.5

Pin Map



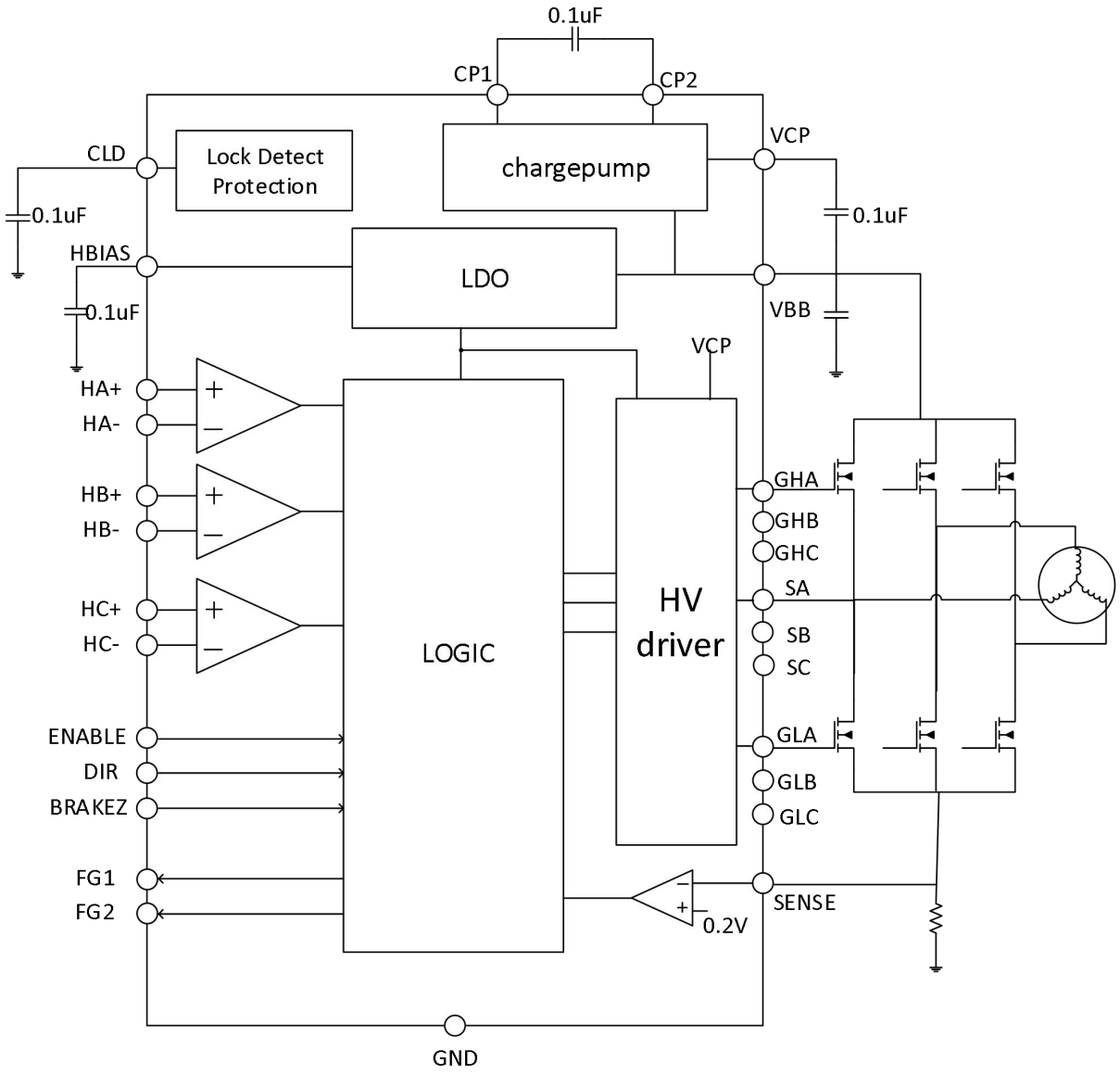
Pin Description

Pin.num	Pin Name	I/O	Pin Function
1	HA+	I	HALL A Phase positive input
2	HA-	I	HALL A Phase negative input
3	HB+	I	HALL B Phase positive input
4	HB-	I	HALL B Phase negative input
5	HC+	I	HALL C Phase positive input
6	HC-	I	HALL C Phase negative input
7	GND	Gnd	Ground
8	HBIAS	IO	5V Power output
9	CP1	IO	Charge pump 1
10	CP2	IO	Charge pump 2
11	VBB	Power	Power supply
12	VCP	IO	Charge pump capacitor pin
13	SENSE	IO	Current monitoring pin
14	GLC	IO	C Phase lower arm bridge grid drive
15	GLB	IO	B Phase lower arm bridge grid drive
16	GLA	IO	A Phase lower arm bridge grid drive
17	GHC	IO	C Phase up arm bridge grid drive
18	SC	IO	C Phase output
19	GHB	IO	B Phase up arm bridge grid drive
20	SB	Gnd	B Phase output

Pin Description (continued)

Pin.num	Pin Name	I/O	Pin Function
21	GHA	IO	A Phase up arm bridge grid drive
22	SA	IO	A Phase output
23	FG1	O	Speed output pin (3ϕ)
24	FG2	O	Speed output pin (ϕ)
25	CLD	IO	Locked rotor protection external regulating capacitor pin
26	DIR	I	Motor direction pin
27	ENABLE	I	External PWM control pin (low effective)
28	BRAKEZ	I	Brake (low effective)

Block Diagram



Absolute Maximum Ratings

(over operating free-air temperature range, unless otherwise noted)

Symbol	Parameter	Rating	Unit
VBB	Maximum operating voltage	38	V
VHx	Hall input voltage	-0.3~7.0	V
Vin	Logic input voltage	-0.3~7.0	V
Topr	Operating ambient temperature	-40~110	°C
Tjmax	Maximum Junction Temperature	-40~150	°C
Tstg	Storage temperature	-60~150	°C
ESD	Human body model	±3500	V

Electrical Characteristics

(unless otherwise specified, T=25°C, VBB=24V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pin parameters						
supply voltage	V_{BB}	GC4931P	4.7		36	V
Operating current	I_{BB}	f_{PWM}<30kHz,C_{load}=1nF		4	6	mA
		Chargepump On, output off, power saving mode		3.3	3.6	mA
HBIAS Pin voltage	V_{HBIAS}	0<I_{HBIAS}<24	5.1	5.2	5.3	V
HBIAS current	I_{HBIAS}		35			mA
FG Support voltage	V_{FG}		0		6	V
FG Pin current	I_{FG}		0		14	mA
Logic input						
High level input voltage	V_{IN1}		2		V_{HBIAS}	V
Low level input voltage	V_{IN0}		0		0.8	V
Input anti shake hysteresis	T_{glitch}	ENABLE, BRAKEZ, DIR	700	1000	1300	ns
ENABLE Power saving mode delay	Td_{enable}	ENABLE High to output Off	2.1	3	3.9	ms
HBIAS Wake up time	Td_{HBIAS}	HBIAS cap 0.1uF		15	25	us
Output driver module						
High gate output	$V_{GS(H)}$	I_{GATE}=2mA		5.2		V
Low gate output	$V_{GS(L)}$	I_{GATE}=2mA		5.3		V
Gate drive current	I_{GATE}		20	30		mA
Gate drive pull-down resistance	R_{GATE}		10	28	40	Ω
Dead Time	T_{dead}	ID=-1A	0.7	1.0	1.3	us
Current limiting threshold voltage	V_{REF}	ID=1A		200		mV
Fixed attenuation period	T_{off}		18	25	37	us
Protection module						
Over temperature shutdown	TSD		155	170	185	°C
Hysteresis	ΔTSD			20		°C
VCP undervoltage protection voltage	ΔV_{CPUV}	be relative to VBB	4.6		6	V
Locked protection time	T_{LOCK}	CLD capacitance 0.1uF	1.5	2	2.5	s
VBB overvoltage protection	V_{BBOV}	VBB overvoltage protection point	28.5	29	29.5	V
VBB overvoltage protection hysteresis	ΔV_{BBOV}	VBB overvoltage protection hysteresis		2		V

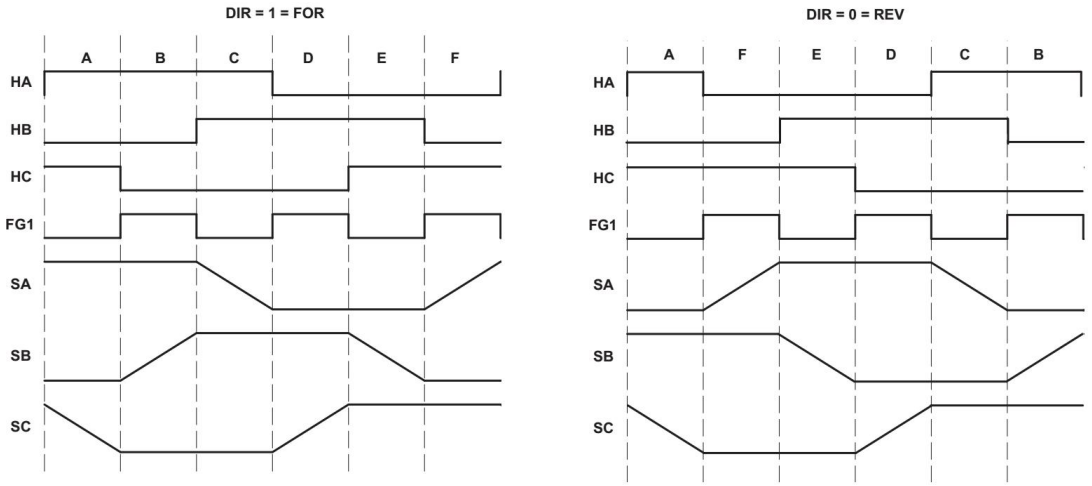
Electrical Characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
HALL amplifier						
Input current	I_{HALL}	VIN=0.2~3.5V	-1	0	1	uA
Common mode voltage	V_{CMR}	Input CMR	0.2		3.5	V
Hall input sensitivity	V_{HALL}	Min differential input voltage		±10		mV
Hall input hysteresis	Vth		5	20	40	mV
Abnormal pulse filtering	T_{pulse}			2		us
FG1/FG2						
On resistance	V_{FGsat}	I_{FG}=2mA			0.5	V
Leakage current	I_{FGlkg}	V_{FG}=5V			1	uA

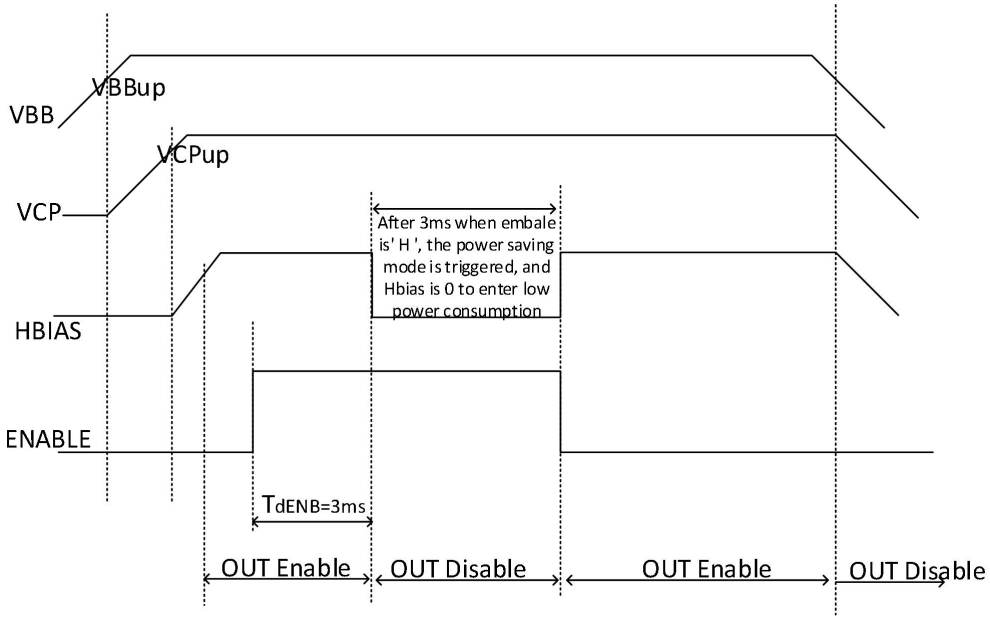
Function Description

1. Logic truth table (x is arbitrary, Z is high resistance state)

Condition		Inputs					Resulting Pre-Driver Outputs						Motor Output		
		HA	HB	HC	BRAKEZ	ENB	GHA	GLA	GHB	GLB	GHC	GLC	A	B	C
DIR = 1 (Forward)	A	+	–	+	HI	LO	HI	LO	LO	HI	LO	LO	HI	LO	Z
	B	+	–	–	HI	LO	HI	LO	LO	LO	LO	HI	HI	Z	LO
	C	+	+	–	HI	LO	LO	LO	HI	LO	LO	HI	Z	HI	LO
	D	–	+	–	HI	LO	LO	HI	HI	LO	LO	LO	LO	HI	Z
	E	–	+	+	HI	LO	LO	HI	LO	LO	HI	LO	LO	Z	HI
	F	–	–	+	HI	LO	LO	LO	LO	HI	HI	LO	Z	LO	HI
DIR = 0 (Reverse)	A	+	–	+	HI	LO	LO	HI	HI	LO	LO	LO	LO	HI	Z
	F	–	–	+	HI	LO	LO	LO	HI	LO	LO	HI	Z	HI	LO
	E	–	+	+	HI	LO	HI	LO	LO	LO	LO	HI	HI	Z	LO
	D	–	+	–	HI	LO	HI	LO	LO	HI	LO	LO	HI	LO	Z
	C	+	+	–	HI	LO	LO	LO	LO	HI	HI	LO	Z	LO	HI
	B	+	–	–	HI	LO	LO	HI	LO	LO	HI	LO	LO	Z	HI
Fault*		+	+	+	HI	X	LO	LO	LO	LO	LO	LO	Z	Z	Z
Fault*		–	–	–	HI	X	LO	LO	LO	LO	LO	LO	Z	Z	Z
Brake*		X	X	X	LO	X	LO	HI	LO	HI	LO	HI	LO	LO	LO



2. Power on Sequence & power saving mode sequence diagram



3. Current limit Regulation

Load current is regulated by an internal fixed off-time PWM control circuit. When the outputs of the full bridge are turned on, current increases in the motor winding until it reaches a value, Itrip, given by:

Itrip = 200mV / Rsense

When Itrip is reached, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate for the fixed off-time period.

4. ENABLE Logic

The ENABLE input terminal allows external PWM. ENABLE low turns on the selected sink-source pair. ENABLE high switches off the appropriate drivers and the load current decays. If ENABLE is held low, the current will rise until it reaches the level set by the internal current control circuit. Typically PWM frequency is in 20 kHz to 30 kHz range. If the ENABLE high pulse width exceeds 3 ms, the gate outputs are disabled. The ENABLE logic is summarized in the following table:

ENABLE	Output drive tube status	Motor drive status
0	Open	Effective
1	Upper arm bridge off	Slow attenuation band synchronous rectifier
1(Duration greater than 3ms)	Turn off	Invalid

5. PWM Blank time

When a source driver turns on, a current spike occurs due to the reverse recovery currents of the clamp diodes as well as switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source Enable latch, the sense comparator is blanked. The blanking timer runs after the off-time counter completes, in order to provide the blanking function. The blanking timer is reset when ENB is chopped or DIR is changed. With external PWM control, a DIR change or an ENB on triggers the blanking function. The duration is fixed at 1.5 μs.

6. Synchronous Rectification

When a PWM-off cycle is triggered, either by a chop command on ENABLE or by an internal fixed off-time cycle, load current recirculates. The GC4931P synchronous rectification feature turns on the appropriate MOSFETs during the current decay, and effectively shorts out the body diodes with the low RDS(on) driver. This lowers power dissipation significantly and can eliminate the need for external Schottky diodes.

7. Brake Mode

A logic low on the BRAKEZ pin activates Brake mode. A logic high allows normal operation. Braking turns on all three sink drivers, effectively shorting out the motor-generated BEMF. The BRAKEZ input overrides the ENABLE input and also the Lock Detect function.

It is important to note that the internal PWM current control circuit does not limit the current when braking, because the current does not flow through the sense resistor. The maximum current can be approximated by VBEMF / RLOAD. Care should be taken to insure that the maximum ratings of the GC4931P are not exceeded in the worse case braking situation, high speed and high inertial load.

8. HBIAS Function

The chip has a built-in LDO output of 5.2v and a maximum current of 30mA for Hall IC.

9. Standby Mode

To prevent excessive power dissipation due to the current draw of the external Hall elements, Standby mode turns off the HBIAS output voltage. Standby mode is triggered by holding ENABLE high for longer than 3 ms. Note that Brake mode overrides Standby mode, so hold the BRAKEZ pin high in order to enter Standby mode.

10. Charge Pump

The internal charge pump is used to generate a supply above VBB to drive the high-side MOSFETs. The voltage on the VCP pin is internally monitored, and in case of a fault condition, the outputs of the device are disabled.

11. Fault Shutdown

In the event of a fault due to excessive junction temperature or due to low voltage on VCP or VBB, the outputs of the device are disabled until the fault condition is removed. At power-up the UVLO circuit disables the drivers.

12. Overvoltage Protection

VBB is monitored to determine if a hazardous voltage is present due to the motor generator pumping up the supply bus. When the voltage exceeds VBBOV , the synchronous rectification feature is disabled.

13. Overtemperature Protection

If chip temperature exceeds approximately 170°C, the Thermal Shutdown function will disable the outputs until the internal temperature falls below the 18°C hysteresis.

However, because the over temperature protection is activated only when the chip junction temperature exceeds the set value, it does not guarantee that the product will be protected from damage with this circuit.

14. Hall State Reporting

The FG1 and FG2 pins are open drain output pins to reflect the internal hall working state. FG1 outputs the change of Hall signal each time. FG2 outputs the change of HAx.

15. Lock Detect Function

The IC will evaluate a locked rotor condition under either of these two different conditions:

1. The FG1 signal is not consistently changing.
2. The proper commutation sequence is not being followed. The motor can be locked in a condition in which it toggles between two specific Hall device states.

When it is detected that the duration of the locked rotor condition exceeds tlock, the output drive will be closed and the locked rotor condition will be locked. It can be unlocked only when the following conditions occur:

1. DIR rising or falling edge
2. ENB continuous high exceeds tlock/2
3. VBB elimination of low voltage detection (power on again)

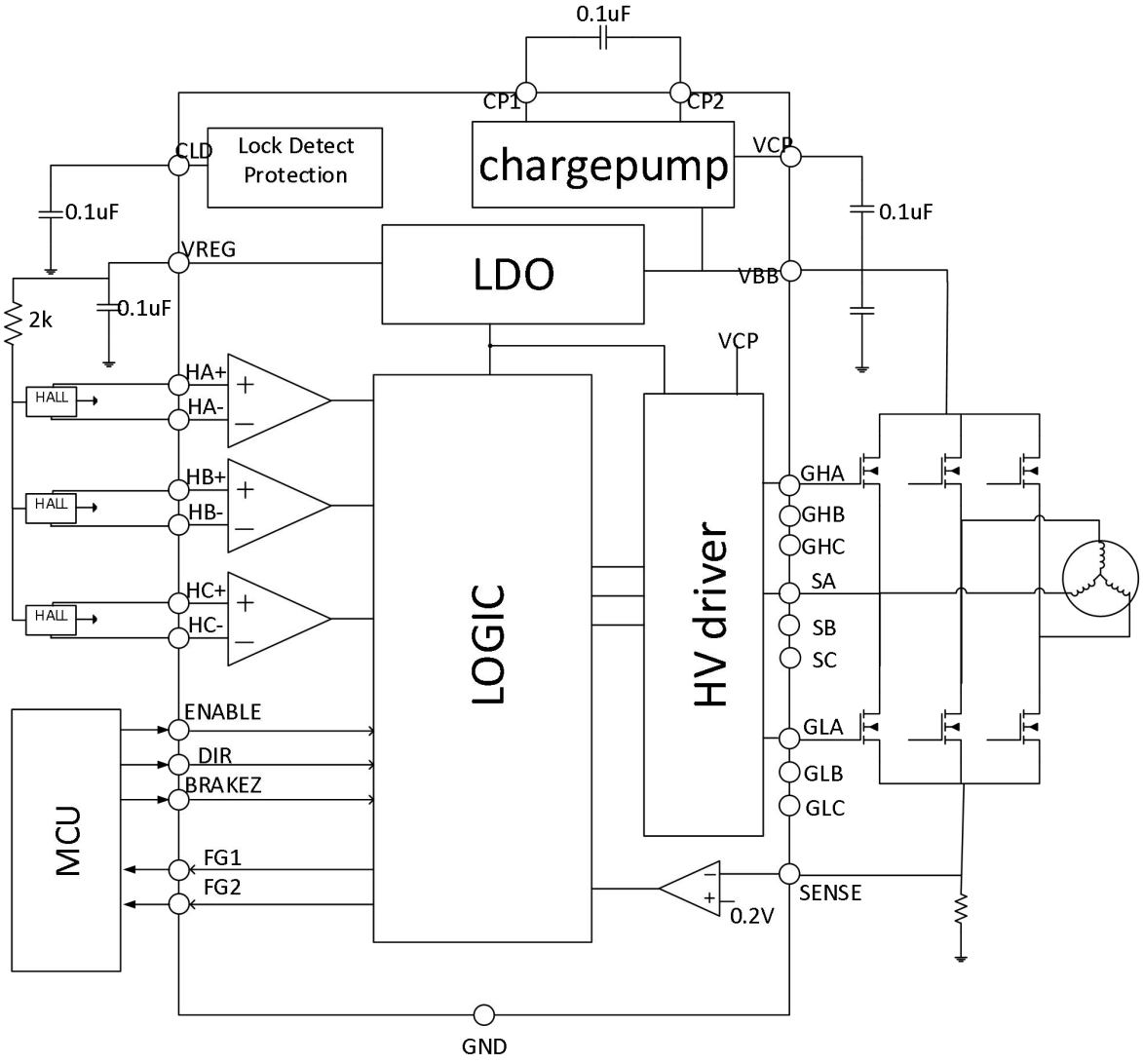
tlock is determined by the external capacitance of CLD pin. CLD pin is the external capacitance pin of 1.67v peak to peak triangular wave oscillator. The calculation formula of tlock is as follows:

tlock = Ccld x 20 s/uF

When the CLD is short circuited to the ground, the locked rotor protection function is closed.

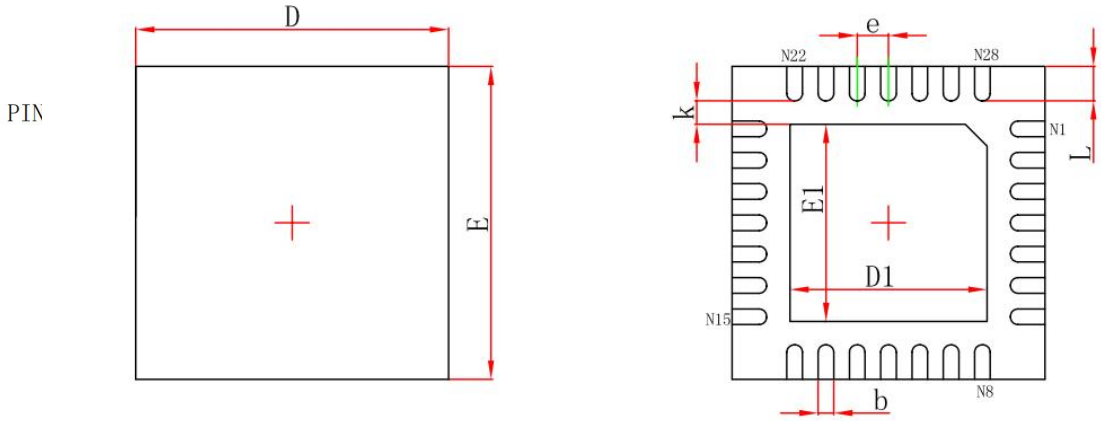
When in braking mode, the stall detection counter is turned off.

Typical Application

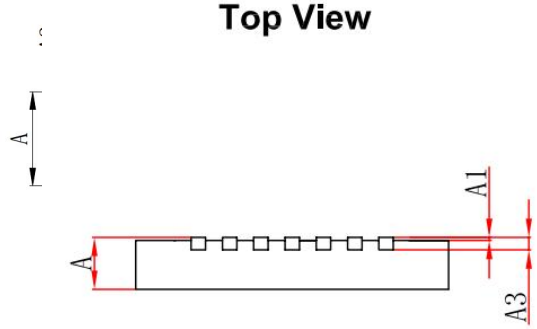


Package Information

QFNWB5x5-28L(P0.5T0.75/0.8) **UNIT: mm**



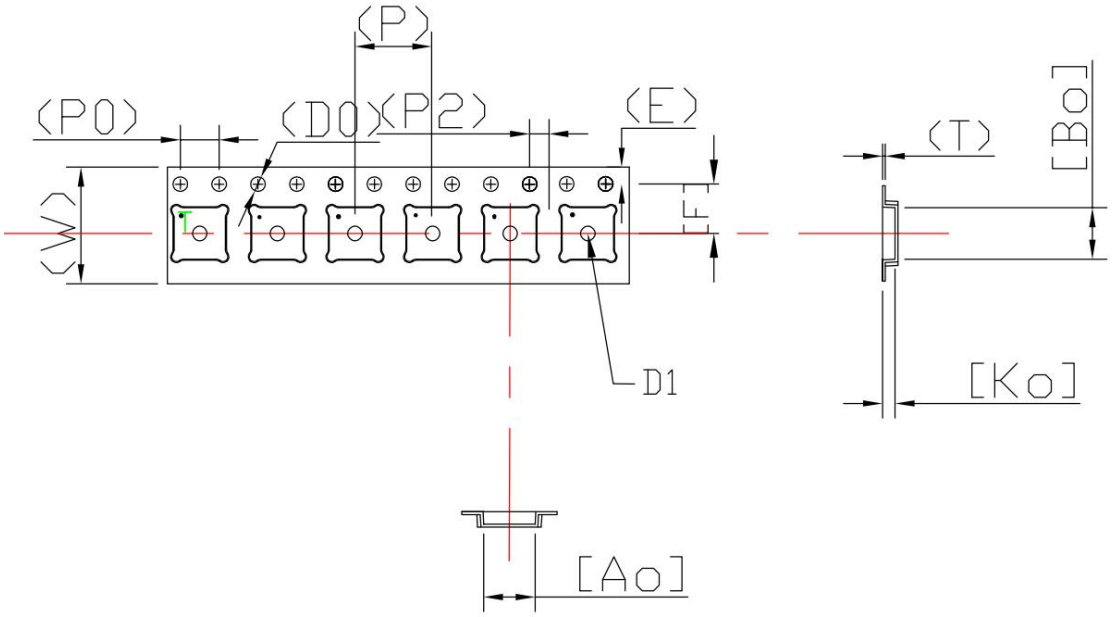
Top View **Bottom View**



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.900	5.100	0.193	0.201
E	4.900	5.100	0.193	0.201
D1	3.050	3.250	0.120	0.128
E1	3.050	3.250	0.120	0.128
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.450	0.650	0.018	0.026

Carrier Tape and Reel Information



NOTES:

1. 10 sprocket hole pitch cumulative tolerance ± 0.20 mm.
   每10个料带链孔径累计公差为±0.20毫米。
2. Carrier camber not to exceed 1mm in 100 mm.
   料带弯曲每100毫米不可超过1毫米。
3. A_o and B_o measured on a plane 0.3 mm above the bottom of the pocket.
   A0和B0在同一平面量测且距离压缩带底部0.3毫
4. All scope meet EIA-481-D requirements.
   所有尺寸符合EIA-481-D标准要求。
5. Material: Black PS.
   材料：黑色 PS 。
6. Thickness: 0.30± 0.05 mm.
   厚度：0.30±0.05毫米。
7. Packing lenght per 13" reel : 40.6 Meters.
   13"纸盘包装长度为：40.6
8. Component load per 13" reel : 5075 pcs.
   13"胶盘可包装：5075 pcs。

ITEM	W	A0	A1	B0	B1	K0	K1	E	F	P	P0	P2	D0	D1	T
DIM	12.0	5.30	0.00	5.30	0.00	1.30	0.00	1.75	5.50	8.0	4.0	2.0	1.50	1.50	0.30
TOLE	+0.30 −0.30	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	+0.10 −0.00	+0.10 −0.00	±0.05

Devices Per Unit

Device	Per Tray	Per Box	Per Case
GC4931P	5,000	10,000	80,000