1. DESCRIPTION

The XL33290 is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing in automotive diagnostic applications. It is designed to interface between the vehicle's on-board microcontroller and systems off-board the vehicle via the special ISO K line. The XL33290 is designed to meet the Diagnostic Systems ISO9141 specification. The device's K line bus driver's output is fully protected against bus shorts and overtemperature conditions.

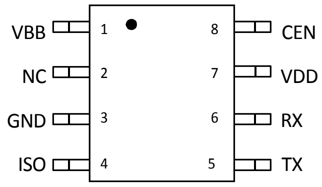
The XL33290 derives its robustness to temperature and voltage extremes by being built on a SMARTMOS process, incorporating CMOS logic, bipolar/MOS analog circuitry, and DMOS power FETs. Although the XL33290 was principally designed for automotive applications, it is suited for other serial communication applications. It is parametrically specified over an ambient temperature range of-40°C ≤ TA ≤ 85°C and 8.0 V ≤ VBB ≤ 18 V supply. The economical SOP8 surface-mount plastic package makes the XL33290 very cost effective.

2. FEATURES

- Operates Over Wide Supply Voltage of 8.0 to 18V
- Operating Temperature of -40 to 85°C
- Interfaces Directly to Standard CMOS Microprocessors
- ISO K Line Pin Protected Against Shorts to Ground
- Thermal Shutdown with Hysteresis
- ISO K Line Pin Capable of High Currents
- ISO K Line Can Be Driven with up to 10 nF of Parasitic Capacitance
- 8.0 kV ESD Protection Attainable with Few Additional Components
- Standby Mode: No VBat Current Drain with VDD at 5.0 V
- Low Current Drain During Operation with VDD at 5.0 V

3. PIN CONFIGURATIONS AND FUNCTIONS

XL33290



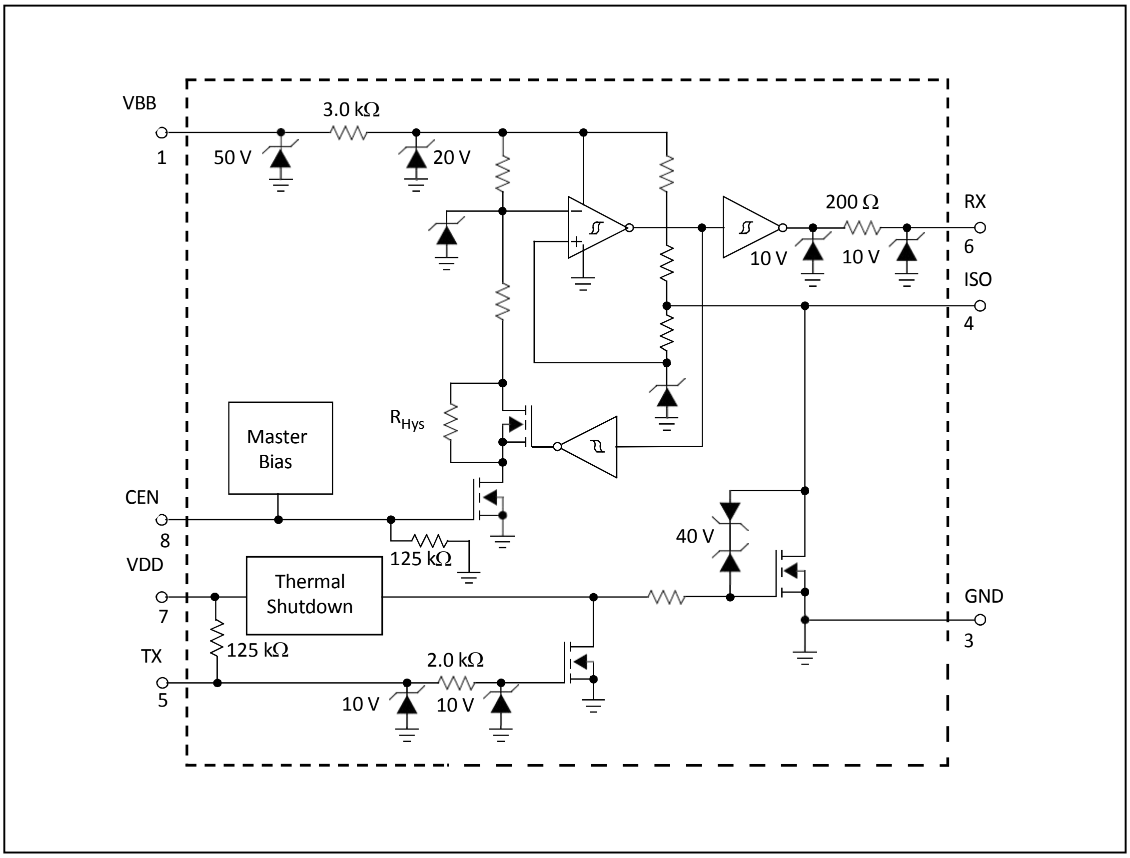
SOP8 (TOP VIEW)

Pin Functions

Pin Number	Pin Name	Definition
1	VBB	Battery power through external resistor and diode.
2	NC	Not to be connected. [1]
3	GND	Common signal and power return.
4	ISO	Bus connection.
5	TX	Logic level input for data to be transmitted on the bus.
6	RX	Logic output of data received on the bus.
7	VDD	Logic power source input.
8	CEN	Chip enable. Logic “1” for active state. Logic “0” for sleep state.

[1] Notes: NC pins should not have any connections made to them. NC pins are not guaranteed to be open circuits.

4. FUNCTIONAL BLOCK DIAGRAM



Block Diagram

5. SPECIFICATIONS

5.1. Absolute Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
V_{DD} DC Supply Voltage	V_{DD}	-0.3 to 7.0	V
VBB Load Dump Peak Voltage	$V_{BB(LD)}$	45	V
ISO Pin Load Dump Peak Voltage [2]	V_{ISO}	40	V
ISO Short Circuit Current Limit	$I_{ISO(LIM)}$	1.0	A
ESD Voltage [3] Human Body Model [4] Machine Model [4]	V_{ESD1} V_{ESD2}	±2000 ±200	V
ISO Clamp Energy [5]	E_{clamp}	10	mJ
Storage Temperature	T_{stg}	-55 to +150	°C
Operating Case Temperature	T_C	-40 to +85	°C
Operating Junction Temperature	T_J	-45 to +125	°C
Power Dissipation T_A = 25°C	P_D	0.8	W
Peak Package Reflow Temperature During Reflow [6]	T_{PPRT}	-	°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	150	°C/W

Notes

[2] Device will survive double battery jump start conditions in typical applications for 10 minutes duration, but is not guaranteed to remain within specified parametric limits during this duration.

[3] ESD data available upon request.

[4] ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (CZAP = 200 pF, RZAP = 0 Ω).

[5] Nonrepetitive clamping capability at 25°C.

[6] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

5.2. Static Electrical Characteristics

Characteristics noted under conditions of 4.75 V ≤ VDD ≤ 5.25 V, 8.0 V ≤ VBB ≤ 18 V, -40°C ≤ TC ≤ 85°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER AND CONTROL					
V_{DD} Sleep State Current T_X = 0.8 V_{DD}, CEN = 0.3 V_{DD}	$I_{DD(SS)}$	–	–	0.1	mA
V_{DD} Quiescent Operating Current T_X = 0.2 V_{DD}, CEN = 0.7 V_{DD}	$I_{DD(Q)}$	–	–	1.0	mA
V_{BB} Sleep State Current V_{BB} = 16 V, T_X = 0.8 V_{DD}, CEN = 0.3 V_{DD}	$I_{BB(SS)}$	–	–	50	µA
V_{BB} Quiescent Operating Current T_X = 0.2 V_{DD}, CEN = 0.7 V_{DD}	$I_{BB(Q)}$	–	–	1.0	mA
Chip Enable Input High-Voltage Threshold [7] Input Low-Voltage Threshold [8]	$V_{IH(CEN)}$ $V_{IL(CEN)}$	0.7 V_{DD} –	– –	– 0.3 V_{DD}	V
Chip Enable Pull-Down Current [9]	$I_{PD(CEN)}$	2.0	–	40	µA
T_X Input Low-Voltage Threshold R_{ISO} = 510 Ω [10]	$V_{IL(Tx)}$	–	–	0.3 x V_{DD}	V
T_X Input High-Voltage Threshold R_{ISO} = 510 Ω [11]	$V_{IH(Tx)}$	0.7 x V_{DD}	–	–	V
T_X Pull-Up Current [12]	$I_{PU(Tx)}$	-40	–	-2.0	µA
R_X Output Low-Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}, R_X Sinking 1.0 mA	$V_{OL(Rx)}$	–	–	0.2 V_{DD}	V
R_X Output High-Voltage Threshold R_{ISO} = 510 Ω, T_X = 0.8 V_{DD}, R_X Sourcing 250 µA	$V_{OH(Rx)}$	0.8 V_{DD}	–	–	V
Thermal Shutdown [13]	T_{LIM}	150	170	–	°C

Notes

[7] When IBB transitions to >100 µA.

[8] When IBB transitions to <100 µA.

[9] Enable pin has an internal current pull-down. Pull-down current is measured with CEN pin at 0.3 V_{DD}.

[10] Measured by ramping TX down from 0.7 V_{DD} and noting TX value at which ISO falls below 0.2 V_{BB}.

[11] Measured by ramping TX up from 0.3 V_{DD} and noting the value at which ISO rises above 0.9 V_{BB}.

[12] Tx pin has internal current pull-up. Pull-up current is measured with TX pin at 0.7 V_{DD}.

[13] Thermal Shutdown performance (T_{LIM}) is guaranteed by design but not production tested.

Static Electrical Characteristics (Continued)

Characteristics noted under conditions of 4.75 V ≤ VDD ≤ 5.25 V, 8.0 V ≤ VBB ≤ 18 V, -40°C ≤ TC ≤ 85°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ISO I/O					
R_{ISO} = 0 Ω, T_X = 0.8 V_{DD} [14]	$V_{IL(ISO)}$	–	–	0.4 x V_{BB}	V
Input High Voltage Threshold R_{ISO} = 0 Ω, T_X = 0.8 V_{DD} [15]	$V_{IH(ISO)}$	0.7 x V_{BB}	–	–	V
Input Hysteresis [16]	$V_{Hys(ISO)}$	0.05 x V_{BB}	–	0.1 x V_{BB}	V
Internal Pull-Up Current R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}, V_{ISO} = 9.0 V, V_{BB} = 18 V	$I_{PU(ISO)}$	-5.0	–	-140	μA
Short Circuit Current Limit [17] R_{ISO} = 0 Ω, T_X = 0.4 V_{DD}, V_{ISO} = V_{BB}	$I_{SC(ISO)}$	50	–	1000	mA
Output Low Voltage R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}	$V_{OL(IS)}$	–	–	0.1 x V_{BB}	V
Output High Voltage R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}	$V_{OH(IS)}$	0.95 x V_{BB}	–	–	V

Notes

[14] ISO ramped from 0.8 V_{BB} to 0.4 V_{BB}, Monitor R_X, Value of ISO voltage at which RX transitions to 0.3 V_{DD}.

[15] ISO ramped from 0.4 V_{BB} to 0.8 V_{BB}, Monitor R_X, Value of ISO voltage at which RX transitions to 0.7 V_{DD}.

[16] Input Hysteresis, $V_{Hys(ISO)} = V_{IH(ISO)} - V_{IL(ISO)}$.

[17] ISO has internal current limiting.

5.3. Dynamic Electrical Characteristics

Characteristics noted under conditions of 4.75 V ≤ VDD ≤ 5.25 V, 8.0 V ≤ VBB≤ 18 V, -40°C ≤ TC ≤ 85°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Fall Time [18] R_{ISO} = 510 Ω to V_{BB}, C_{ISO} = 10 nF to Ground	$t_{fall(ISO)}$	–	–	2.0	μs
ISO Propagation Delay [19] High to Low: R_{ISO} = 510 Ω, C_{ISO} = 500 pF [20] Low to High: R_{ISO} = 510 Ω, C_{ISO} = 500 pF [21]	$t_{PD(ISO)}$	– –	– –	2.0 2.0	μs

Notes

[18] Time required ISO voltage to transition from 0.8 V_{BB} to 0.2 V_{BB}.

[19] Changes in the value of C_{ISO} affect the rise and fall time but have minimal effect on Propagation Delay.

[20] Step T_X voltage from 0.2 V_{DD} to 0.8 V_{DD}. Time measured from $V_{IH(ISO)}$ until V_{ISO} reaches 0.3 V_{BB}.

[21] Step T_X voltage from 0.8 V_{DD} to 0.2 V_{DD}. Time measured from $V_{IL(ISO)}$ until V_{ISO} reaches 0.7 V_{BB}.

6. TYPICAL APPLICATIONS

6.1. INTRODUCTION

The XL33290 is a serial link bus interface device conforming to the ISO 9141 physical bus specification. The device was designed for automotive environment usage compliant with On-Board Diagnostic (OBD) requirements set forth by the California Air Resources Board (CARB) using the ISO K line. The device does not incorporate an ISO L line. It provides bi- directional half-duplex communications interfacing from a microcontroller to the communication bus. The XL33290 incorporates circuitry to interface the digital translations from 5.0 V microcontroller logic levels to battery level logic and from battery level logic to 5.0 V logic levels. The XL33290 is built using Freescale Semiconductor's SMARTMOS process and is packaged in an 8-pin plastic SOP.

6.2. FUNCTIONAL DESCRIPTION

The XL33290 transforms 5.0 V microcontroller logic signals to battery level logic signals and visa versa. The maximum data rate is set by the fall time and the rise time. The fall time is set by the output driver. The rise time is set by the bus capacitance and the pull-up resistors on the bus. The fall time of the XL33290 allows data rates up to 150 kbps using a 30 percent maximum bit time transition value. The serial link interface will remain fully functional over a battery voltage range of 6.0 to 18 V. The device is parametrically specified over a dynamic VBB voltage range of 8.0 to 18 V.

Required input levels from the microcontroller are ratio- metric with the VDD voltage normally used to power the microcontroller. This enhances the XL33290's ability to remain in harmony with the RX and TX control input signals of the microcontroller. The RX and TX control inputs are compatible with standard 5.0 V CMOS circuitry. For fault-tolerant purposes the TX input from the microcontroller has an interna passive pull-up to VDD, while the CEN input has an internal passive pull-down to ground.

A pull-up to battery is internally provided as well as an active data pull-down. The internal active pull-down is current-limit-protected against shorts to battery and further protected by thermal shutdown. Typical applications have reverse battery protection by the incorporation of an external 510Ω pull-up resistor and diode to battery.

Reverse battery protection of the device is provided by using a reverse battery blocking diode ("D" in the Simplified Application Diagram on page 1). Battery line transient protection of the device is provided for by using a 45 V zener and a 500Ω resistor connected to the VBB source as shown in the same diagram. Device ESD protection from the communication lines exiting the module is through the use of the capacitor connected to the VBB device pin and the capacitor used in conjunction with the 27 V zener connected to the ISO pin.

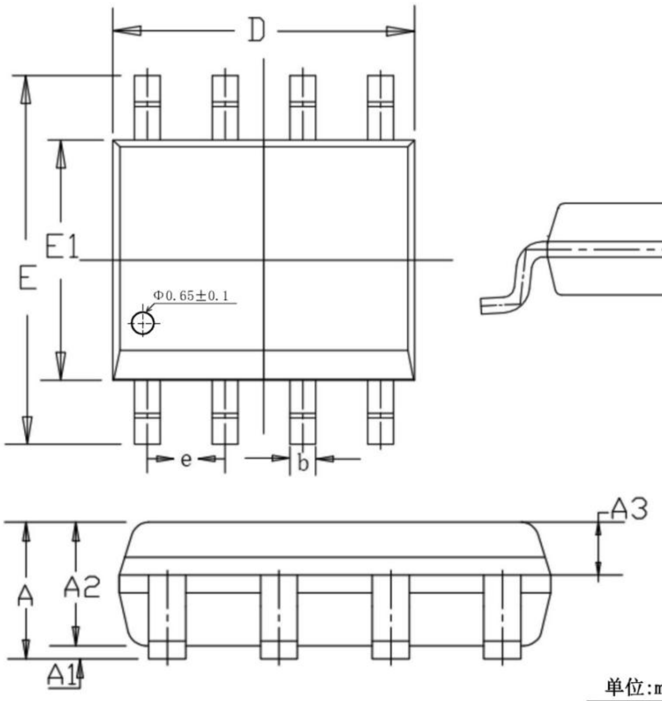
7. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL33290	XL33290	SOP8	4.90 * 3.90	-40 to +85	MSL3	T&R	2500

8. DIMENSIONAL DRAWINGS

SOP8



单位:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
A3	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	–	0.25BSC	–