

# MC14094B

## 8-Stage Shift/Store Register with Three-State Outputs

The MC14094B combines an 8-stage shift register with a data latch for each stage and a 3-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The  $Q_5$  output data is for use in high-speed cascaded systems. The  $Q_8$  output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by 3-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

### Features

- 3-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



ON Semiconductor®

<http://onsemi.com>



SOIC-16  
D SUFFIX  
CASE 751B

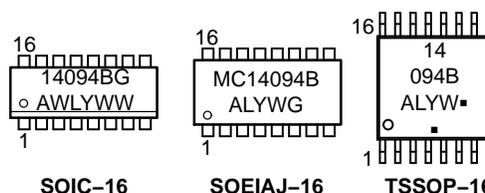


SOEIAJ-16  
F SUFFIX  
CASE 966



TSSOP-16  
DT SUFFIX  
CASE 948F

### MARKING DIAGRAMS



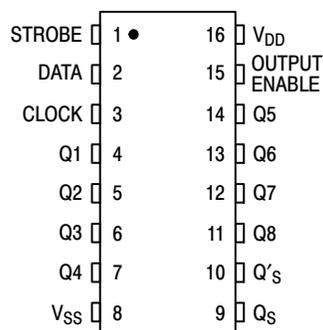
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Indicator

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC14094B

## PIN ASSIGNMENT



## TRUTH TABLE

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q <sub>1</sub>	Q <sub>N</sub>	Q <sub>S</sub> *	Q' <sub>S</sub>
	0	X	X	Z	Z	Q <sub>7</sub>	No Chg.
	0	X	X	Z	Z	No Chg.	Q <sub>7</sub>
	1	0	X	No Chg.	No Chg.	Q <sub>7</sub>	No Chg.
	1	1	0	0	Q <sub>N-1</sub>	Q <sub>7</sub>	No Chg.
	1	1	1	1	Q <sub>N-1</sub>	Q <sub>7</sub>	No Chg.
	1	1	1	No Chg.	No Chg.	No Chg.	Q <sub>7</sub>

Z = High Impedance    X = Don't Care

\* At the positive clock edge, information in the 7th shift register stage is transferred to Q<sub>8</sub> and Q<sub>S</sub>.

## ORDERING INFORMATION

Device	Package	Shipping†
MC14094BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14094BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14094BDR2G*	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14094BDTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14094BDTR2G*	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
MC14094BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MC14094B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
		15	-	0.05	-	0	0.05	-	0.05		
	"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
		15	-	4.0	-	6.75	4.0	-	4.0		
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11	-	11	8.25	-	11	-	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mA <sub>dc</sub>	
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-		
		10	-1.6	-	-1.3	-2.25	-	-0.9	-		
		15	-4.2	-	-3.4	-8.8	-	-2.4	-		
	Sink I <sub>OL</sub>	5.0	0.64	-	0.51	0.88	-	0.36	-	mA <sub>dc</sub>	
		10	1.6	-	1.3	2.25	-	0.9	-		
15	4.2	-	3.4	8.8	-	2.4	-	-			
Input Current	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μA <sub>dc</sub>	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	-	5.0	-	0.005	5.0	-	150	μA <sub>dc</sub>	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (4.1 μA/kHz) f + I <sub>DD</sub>							μA <sub>dc</sub>	
		10	I <sub>T</sub> = (14 μA/kHz) f + I <sub>DD</sub>								
		15	I <sub>T</sub> = (140 μA/kHz) f + I <sub>DD</sub>								
3-State Output Leakage Current	I <sub>TL</sub>	15	-	±0.1	-	±0.0001	±0.1	-	±3.0	μA	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

# MC14094B

## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time (Figure 1) Clock to Serial out QS $t_{PLH}$ , $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 305 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 82 \text{ ns}$ Clock to Serial out Q'S $t_{PLH}$ , $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 350 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 149 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 62 \text{ ns}$ Clock to Parallel out $t_{PLH}$ , $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 375 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 177 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 122 \text{ ns}$ Strobe to Parallel out $t_{PLH}$ , $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 245 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.36 \text{ ns/pF}) C_L + 127 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15  5.0 10 15  5.0 10 15  5.0 10 15	– – –  – – –  – – –  – – –	350 125 95  230 110 75  420 195 135  290 145 100	600 250 190  460 220 150  840 390 270  580 290 200	ns
Output Enable to Output $t_{PHZ}$ , $t_{PZL} = (0.90 \text{ ns/pF}) C_L + 95 \text{ ns}$ $t_{PHZ}$ , $t_{PZL} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PHZ}$ , $t_{PZL} = (0.26 \text{ ns/pF}) C_L + 42 \text{ ns}$ $t_{PLZ}$ , $t_{PZH} = (0.90 \text{ ns/pF}) C_L + 180 \text{ ns}$ $t_{PLZ}$ , $t_{PZH} = (0.36 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLZ}$ , $t_{PZH} = (0.26 \text{ ns/pF}) C_L + 57 \text{ ns}$	$t_{PHZ}$ , $t_{PZL}$  $t_{PLZ}$ , $t_{PZH}$	5.0 10 15  5.0 10 15	– – –  – – –	140 75 55  225 95 70	280 150 110  450 190 140	
Setup Time Data in to Clock	$t_{su}$	5.0 10 15	125 55 35	60 30 20	– – –	ns
Hold Time Clock to Data	$t_h$	5.0 10 15	0 20 20	–40 –10 0	– – –	ns
Clock Pulse Width, High	$t_{WH}$	5.0 10 15	200 100 83	100 50 40	– – –	ns
Clock Rise and Fall Time	$t_{r(cl)}$ $t_{f(cl)}$	5 10 15	– – –	– – –	15 5.0 4.0	$\mu\text{s}$
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	– – –	2.5 5.0 6.0	1.25 2.5 3.0	MHz
Strobe Pulse Width	$t_{WL}$	5.0 10 15	200 80 70	100 40 35	– – –	ns

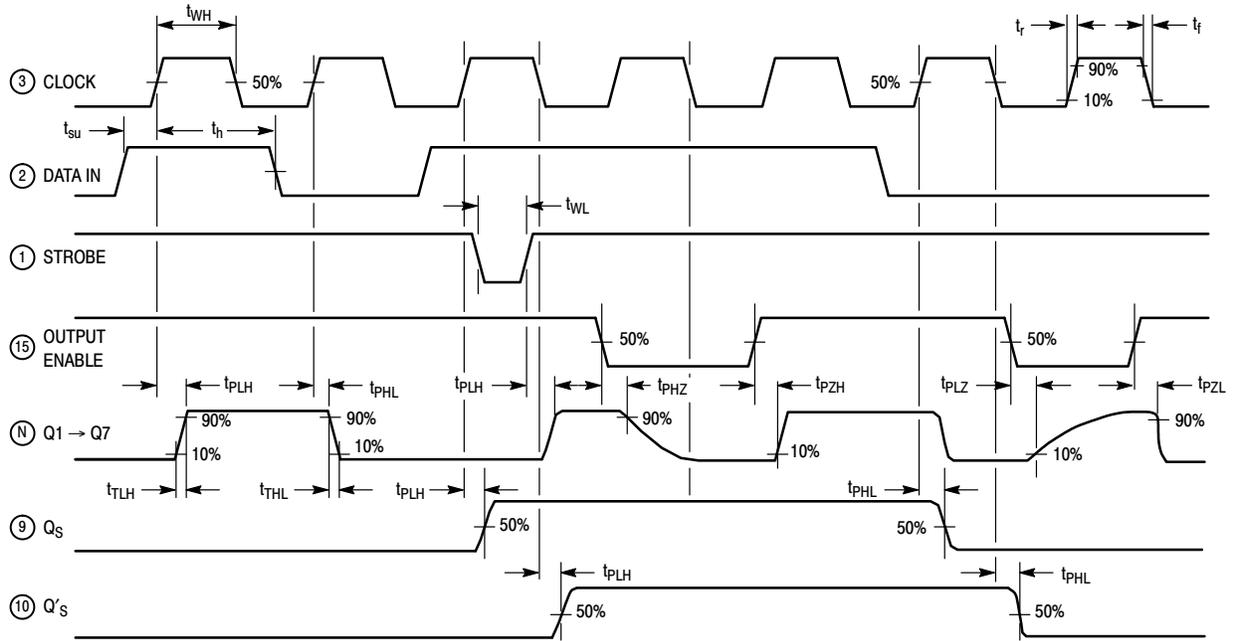
5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



# MC14094B

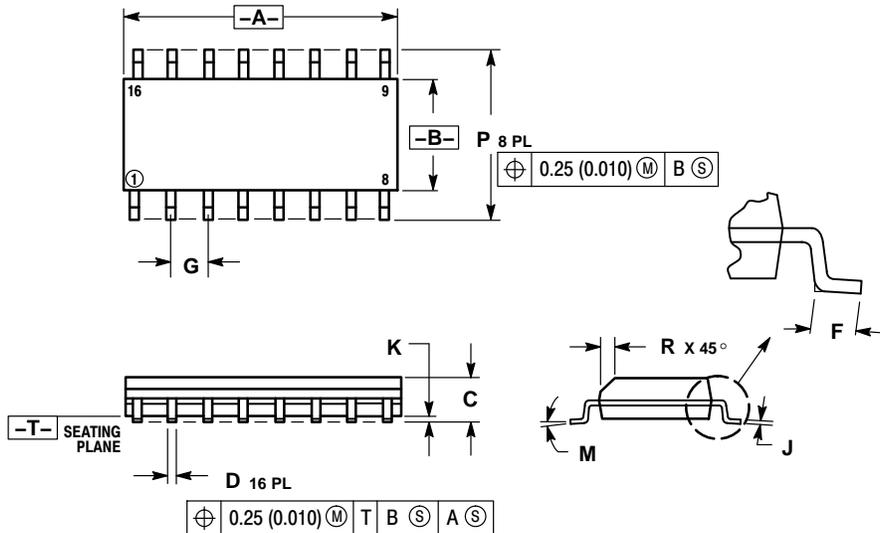
## DYNAMIC TIMING DIAGRAM



# MC14094B

## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE K

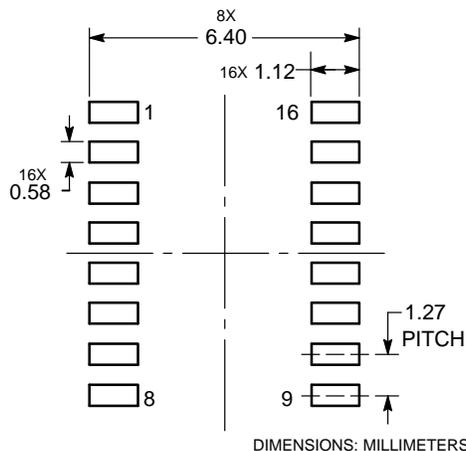


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° - 7°		0° - 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

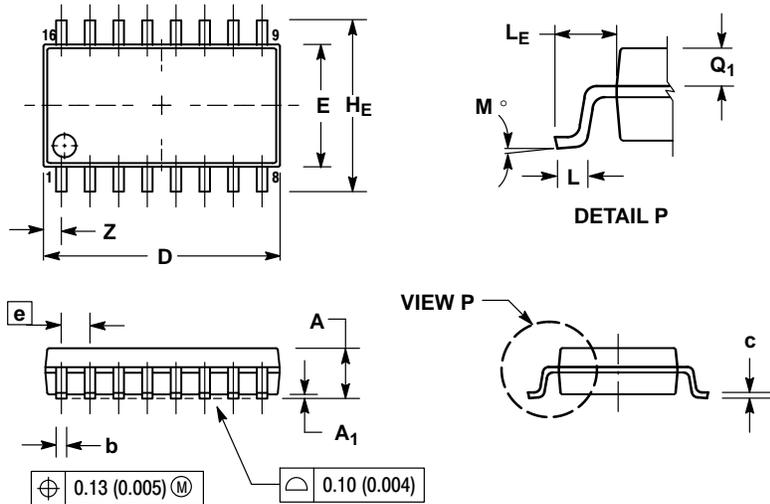
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



# MC14094B

## PACKAGE DIMENSIONS

SOEIAJ-16  
F SUFFIX  
CASE 966  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5817-1050

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative