

## DESCRIPTION

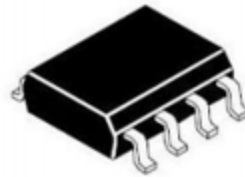
The BDR6307 is a high speed high voltage (600V) driver to control power devices like MOS-transistors or IGBTs in half bridge systems with dependent high and low side referenced output channels. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The device includes an under-voltage detection unit with hysteresis characteristic and prevents power devices against large amount of conduction loss, when voltage margin of gate is not high enough. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT, in the high side configuration which operates up to 600 volts. It is pin and input polarity compatible to IR2101.

## APPLICATIONS

- Appliance motor drives - air conditioners, washing machines, refrigerator, dish washer, Fans
- General purpose inverters
- Electric bike, Electric tools
- Lighting, switching power supply

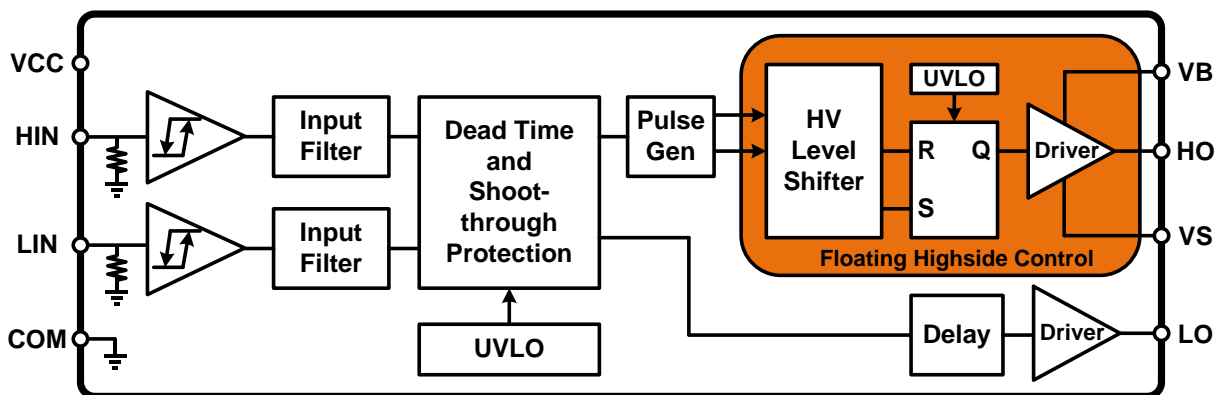
## FEATURES

- Drives two IGBT/MOSFET power devices
- high side channel fully operate up to +600V
- Gate drive supplies from 10V to 20 V per channel
- Under-voltage lockout
- Advanced input filter
- Built-in dead-time protection: 0.5us
- IO+/-: 290/620mA, large sourcing current to bypass miller effect
- Shoot-through (cross-conduction) protection
- 3.3V/5V/15V input logic compatible
- Matched propagation delays for all channels
- Matched dead time
- High side output in phase with HIN input
- Low side output in phase with LIN input
- Tolerant to negative transient voltage, immunity of dv/dt up to 50V/ns
- Low di/dt gate drive for better noised immunity
- -40°C to 125°C operating range
- SOP8L package available
- Lead-free

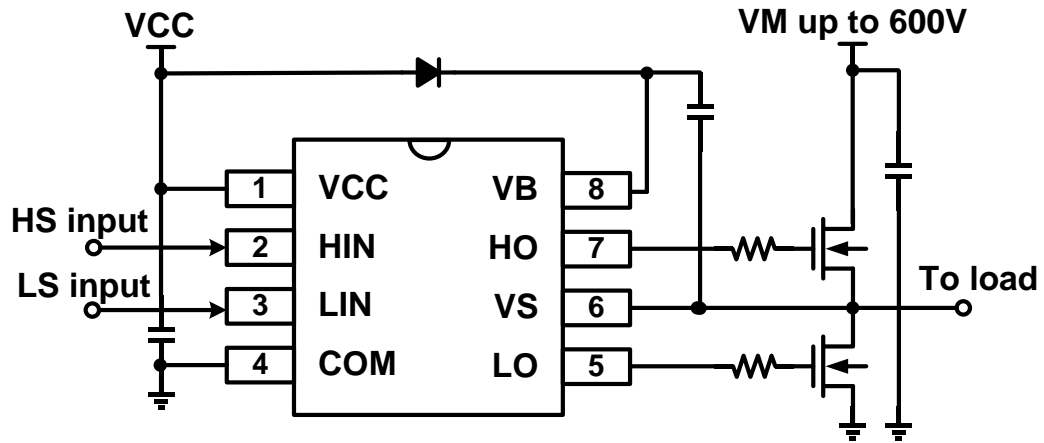


**8-Lead SOIC**

## BLOCK DIAGRAM



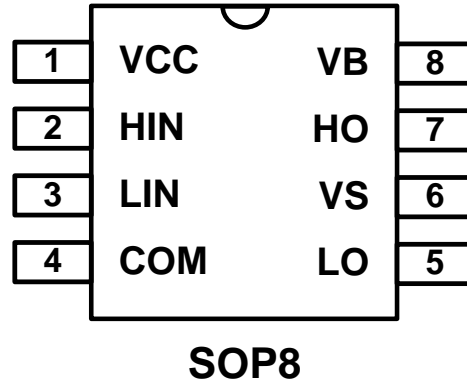
# TYPICAL APPLICATION



## ORDER INFORMATION

Valid Part Number	Package Type	Top Code
BDR6307	8-Pin, SOP, 150 MIL	BDR6307-S

## PIN CONFIGURATION



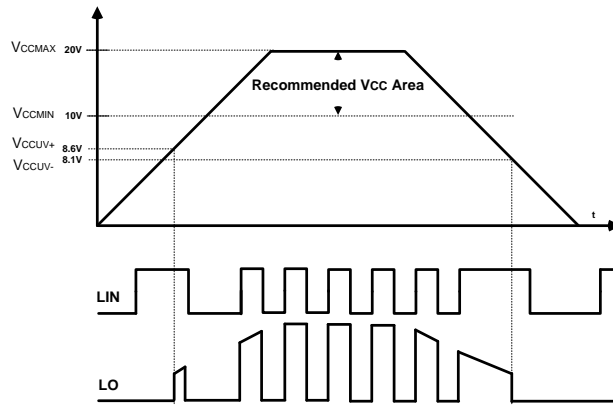
## PIN DESCRIPTION

Pin Name	Description	Pin No.
VCC	Low-side supply voltage	1
HIN	Logic input for high-side gate driver output(HO), in phase	2
LIN	Logic input for low-side gate driver output(LO), in phase	3
COM	Low-side gate drive return	4
LO	Low-side driver output	5
VS	High voltage floating supply return	6
HO	High-side driver output	7
VB	High-side gate drive floating supply	8

# FUNCTION DESCRIPTION

## LOW SIDE POWER SUPPLY

VCC is the low side supply and it provides power both to input logic and to low side output power stage. The built-in under-voltage lockout circuit enables the device to operate at sufficient power on when a typical VCC supply voltage higher than  $V_{CCUV+}=8.6$  is present, shown as Figure1. The IC shuts down the gate drivers outputs, when the VCC supply voltage is below  $V_{CCUV-}=8.1$  V, shown as Figure1. This prevents the external power devices from extremely low gate voltage levels during on-state and therefore from excessive power dissipation.

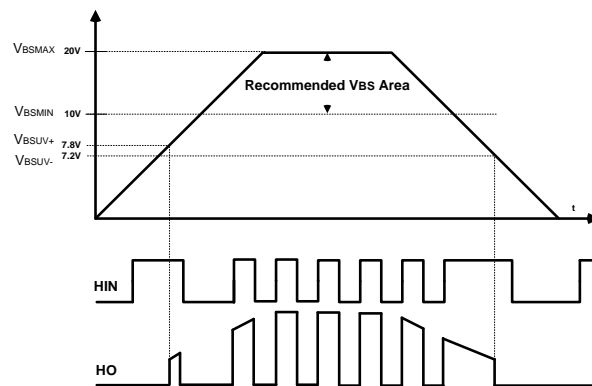


**Figure.1: VCC Supply UVLO Operating Area**

## HIGH SIDE POWER SUPPLY

VB to VS is the high side supply voltage. The totally high side circuitry can float with respect to COM following the external high side power device emitter/source voltage. Due to the internally low power consumption, the whole high side circuitry can be supplied by bootstrap topology connected to VCC, and it can be powered with small bootstrap capacitor tied between PIN VB and PIN VS.

The device operating area as a function of the supply voltage is given in Figure2.

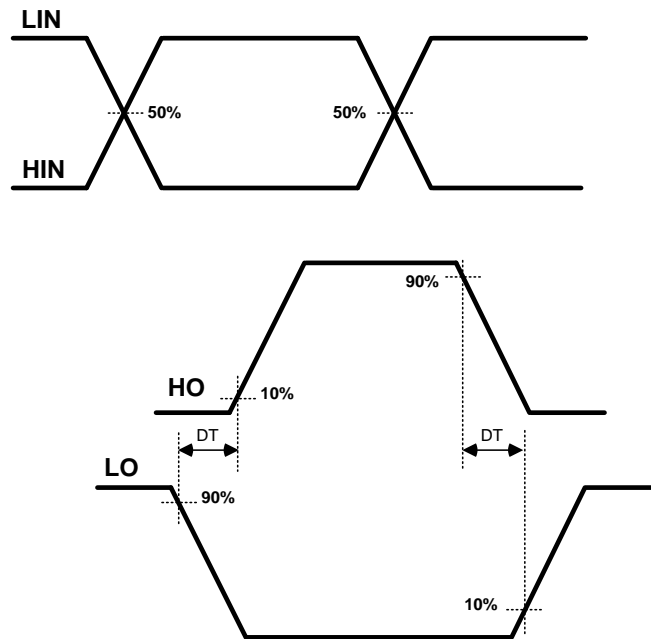


**Figure.2: VBS supply UVLO operating area**

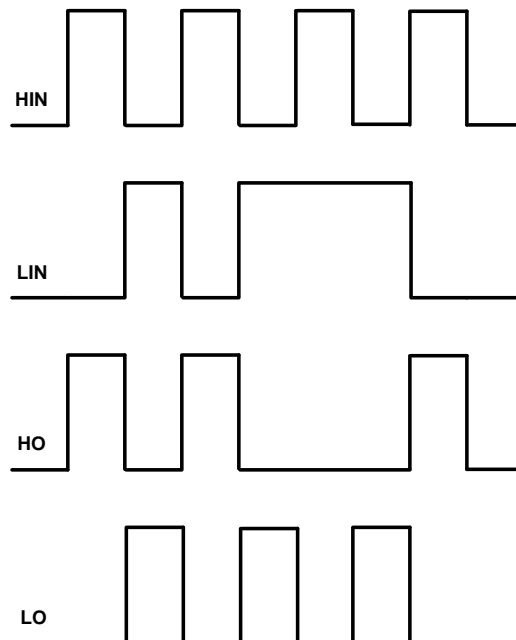
## LOW SIDE AND HIGH CONTROL INPUT LOGIC

The Schmitt trigger threshold level of each input is compatible to LSTTL and CMOS down to 3.3 V. Input Schmitt trigger and advanced noise filter provide beneficial noise rejection to short input pulses.

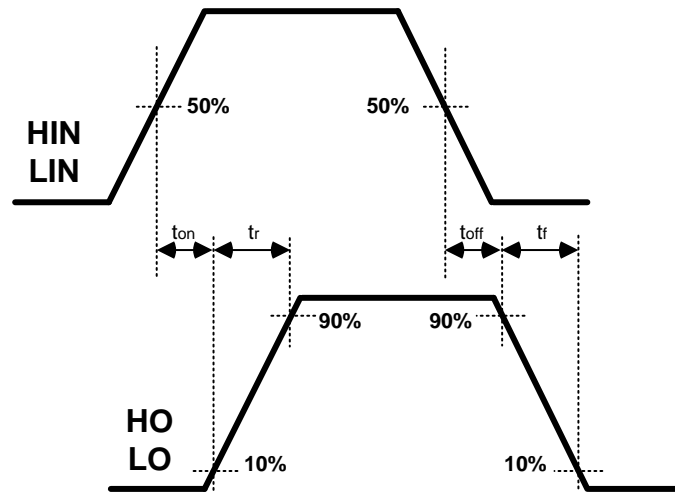
## DEAD TIME



## INPUT/OUTPUT TIMING DIAGRAM



## SWITCHING TIME WAVEFORM DEFINITIONS



## ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device or make the function abnormal. All the voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table.

Parameter	Symbol	Min.	Max.	Units
High-side floating supply voltage	$V_B$	-0.3	625	V
High-side offset voltage	$V_S$	$V_B - 25$	$V_B + 0.3$	
High-side gate driver output voltage	$V_{HO}$	$V_S - 0.3$	$V_S + 0.3$	
Low-side gate driver output voltage	$V_{LO}$	COM-0.3	$V_{CC} + 0.3$	
Logic input voltage(HIN,LIN )	$V_{HIN}$ $V_{LIN}$	-0.3	25	
Low-side supply voltage	$V_{CC}$	-0.3	25	
Allowable offset voltage slew rate	$dV/dT$	-	50	V/ns
Package power dissipation @ $T_A \leq +25^\circ\text{C}$	PD	-	0.625	W
Thermal resistance, junction to ambient	$R_{thJA}$		200	$^\circ\text{C/W}$
Junction temperature	$T_J$	-50	+150	$^\circ\text{C}$
Storage temperature	$T_S$	-40	+150	
Lead temperature (soldering, 10 seconds)	$T_L$	-	300	

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Low-side supply voltage	$V_{CC}$	10	-	20	V
High-side Floating Supply Offset Voltage *1	$V_S$	-6	-	600	
High-side Floating Supply Voltage	$V_B$	$V_S + 10$	-	$V_S + 20$	
High-side gate driver output voltage	$V_{HO}$	$V_S$	-	$V_B$	
Low-side gate driver output voltage	$V_{LO}$	COM	-	$V_{CC}$	
Logic input voltage	$V_{HIN}$ $V_{LIN}$	0	-	5	
IC operating junction temperature	$T_J$	-40	-	+125	$^\circ\text{C}$

\*1: For normal logic operation, it is recommended to keep the  $V_S$  above -6V referenced to COM.

# STATIC ELECTRICAL CHARACTERISTICS

( $V_{CC-COM}$ ) = ( $V_B - V_S$ ) = 15V.  $T_{AMB}$  = 25°C unless otherwise specified; The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Low Side Power Supply Characteristics</b>						
VCC quiescent current	$I_{QVCC}$	$V_{HIN} = 0, V_{LIN} = 0$	-	180	250	$\mu A$
VCC supply under-voltage positive going threshold	$V_{CCUV+}$		7.7	8.6	9.5	V
VCC supply under-voltage negative going threshold	$V_{CCUV-}$		7.2	8.1	9	
VCC supply under-voltage lockout hysteresis	$V_{CCCHYS}$		-	0.5	-	
<b>High Side Floating Power Supply Characteristics</b>						
High side VBS supply under-voltage positive going threshold	$V_{BSUV+}$		6.6	7.8	9	V
High side VBS supply under-voltage negative going threshold	$V_{BSUV-}$		6	7.2	8.4	
High side VBS supply under-voltage lockout hysteresis	$V_{BSUVHYS}$		-	0.6	-	
High side VBS quiescent current	$I_{QBS}$	$V_{BS} = 15V$	-	50	85	$\mu A$
Offset supply leakage current	$I_{LK}$	$V_B = V_S = 600V$ $V_{CC} = 0V$	-	-	10	
<b>Gate Driver Output Section</b>						
Output high short-circuit pulse current	$I_{O+}$	$V_{HO} = V_S = 0,$ $V_{HO} = V_B = 15V,$ $PW < 10\mu s$	-	290	-	mA
Output low short-circuit pulse current	$I_{O-}$	$V_{LO} = COM = 0,$ $V_{LO} = V_{CC} = 15V,$ $PW < 10\mu s$	-	620	-	
High level output voltage drop, $V_{CC} - V_{LO}, V_{BS} - V_{HO}$	$\Delta V_{OH}$	$I_{O+} = 20 mA$	-	0.4	1	V
Low level output voltage drop	$\Delta V_{OL}$	$I_{O-} = 20 mA$	-	0.15	0.3	V
Allowable negative VS pin voltage for COM	$V_{SN}$	Fixed $V_{BS} = 15V$	-6	-	-	V
<b>Logic Input Section</b>						
Logic "1" Input voltage HIN and LIN	$V_{IH}$		2.5	-	-	V
Logic "0" Input voltage HIN and LIN	$V_{IL}$		-	-	0.8	
Input positive going threshold	$V_{IN,TH+}$		-	1.9	-	
Input negative going threshold	$V_{IN,TH-}$		-	1.4	-	
Logic "1" Input bias current	$I_{HIN+}$	$V_{IN} = 5V$	-	50	70	$\mu A$
Logic "0" Input bias current	$I_{HIN-}$	$V_{IN} = 0V$	-	0	1	
Logic "1" Input bias current	$I_{LIN+}$	$V_{IN} = 5V$	-	50	70	
Logic "0" Input bias current	$I_{LIN-}$	$V_{IN} = 0V$	-	0	1	



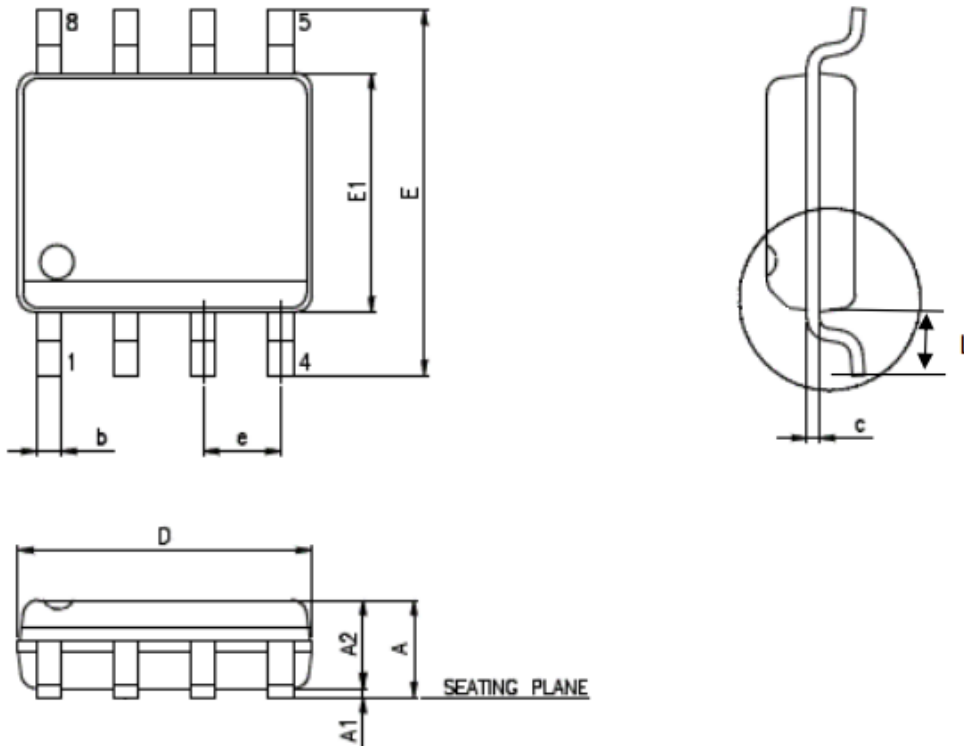
## DYNAMIC ELECTRICAL CHARACTERISTICS

( $V_{CC-COM}$ ) = ( $V_B - V_S$ ) = 15V,  $V_S = COM$ , and  $C_{HO} = C_{LO} = 1nF$  unless otherwise specified,  $T_{AMB} = 25^\circ C$ .

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VCC supply current	$I_{VCCOP}$	$f_{LIN} = 20KHz,$ $f_{HIN} = 20KHz,$	-	1	1.5	mA
Turn-On propagation delay	$t_{ON}$	See switching time waveform definitions	300	500	700	ns
Turn-Off propagation delay	$t_{OFF}$		300	500	700	
Turn-On rise time	$t_R$		-	70	-	
Turn-Off fall time	$t_F$		-	32	-	
Input filter	$t_{fit}$	$V_{IN} = 0$ or 5V	100	250	400	
Dead time	DT	HIN and LIN inputs without external dead time	300	500	700	
Delay matching( $t_{ON}, t_{OFF}$ )	MT	HIN and LIN inputs with external dead time $> 2\mu s$	-	-	50	
Output pulse-width matching	PM	$PW_{IN} = 10\mu s, PM = PW_{OUT} - PW_{IN}$	-	-	50	

# PACKAGE INFORMATION

**8 PINS, SOP, 150MIL**



Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	-	-	1.70
A1	0.00	-	0.15
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
e	1.27 BSC		
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
L	0.40	0.60	1.27

Notes:

1. Refer to JEDEC MS-012 AA
2. Unit: mm

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