MIC2196

400 kHz SOIC-8 Boost Control IC

Features

- 2.9V to 14V Input Voltage Range
- Greater than 90% Efficiency
- 2Ω Output Driver
- 400 kHz Oscillator Frequency
- PWM Current Mode Control
- 0.5 µA Micropower Shutdown
- Programmable UVLO
- Front Edge Blanking
- Cycle-by-Cycle Current Limiting
- Frequency Foldback Short-Circuit Protection
- 8-Lead SOIC Package

Applications

- Step-Up Conversion in Telecom/Datacom Systems
- SLIC Power Supplies
- SEPIC Power Supplies
- Low Input Voltage Flyback and Forward Converters
- Wireless Modems
- Cable Modems
- ADSL Line Cards
- Base Stations
- 1- and 2-Cell Li Ion Battery Operated Equipment

General Description

The MIC2196 is a high efficiency PWM boost control IC housed in a SOIC-8 package. The MIC2196 is optimized for low input voltage applications. With its wide input voltage range of 2.9V to 14V, the MIC2196 can be used to efficiently boost voltages in 3.3V, 5V, and 12V systems, as well as 1- or 2-cell Li Ion battery powered applications. Its powerful 2Ω output driver allows the MIC2196 to drive large external MOSFETs.

The MIC2196 is ideal for space-sensitive applications. The device is housed in the space-saving SOIC-8 package, whose low pin-count minimizes external components. Its 400 kHz PWM operation allows a small inductor and small output capacitors to be used. The MIC2196 can implement all ceramic capacitor solutions.

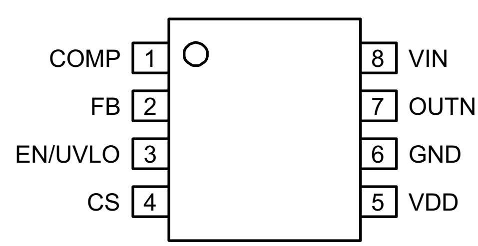
Efficiencies over 90% are achievable over a wide range of load conditions with the MIC2196's PWM boost control scheme. Its fixed frequency PWM architecture also makes the MIC2196 is ideal for noise-sensitive telecommunications applications.

MIC2196 features a low current shutdown mode of 1 µA and programmable undervoltage lockout.

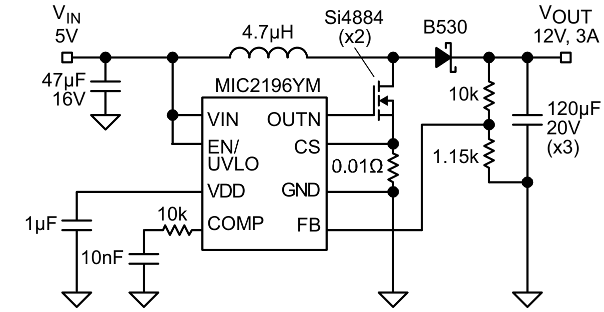
The MIC2196 is available in an 8-lead SOIC package with a junction temperature range from –40°C to +125°C.

Package Type

MIC2196
8-Lead SOIC (M)
(Top View)

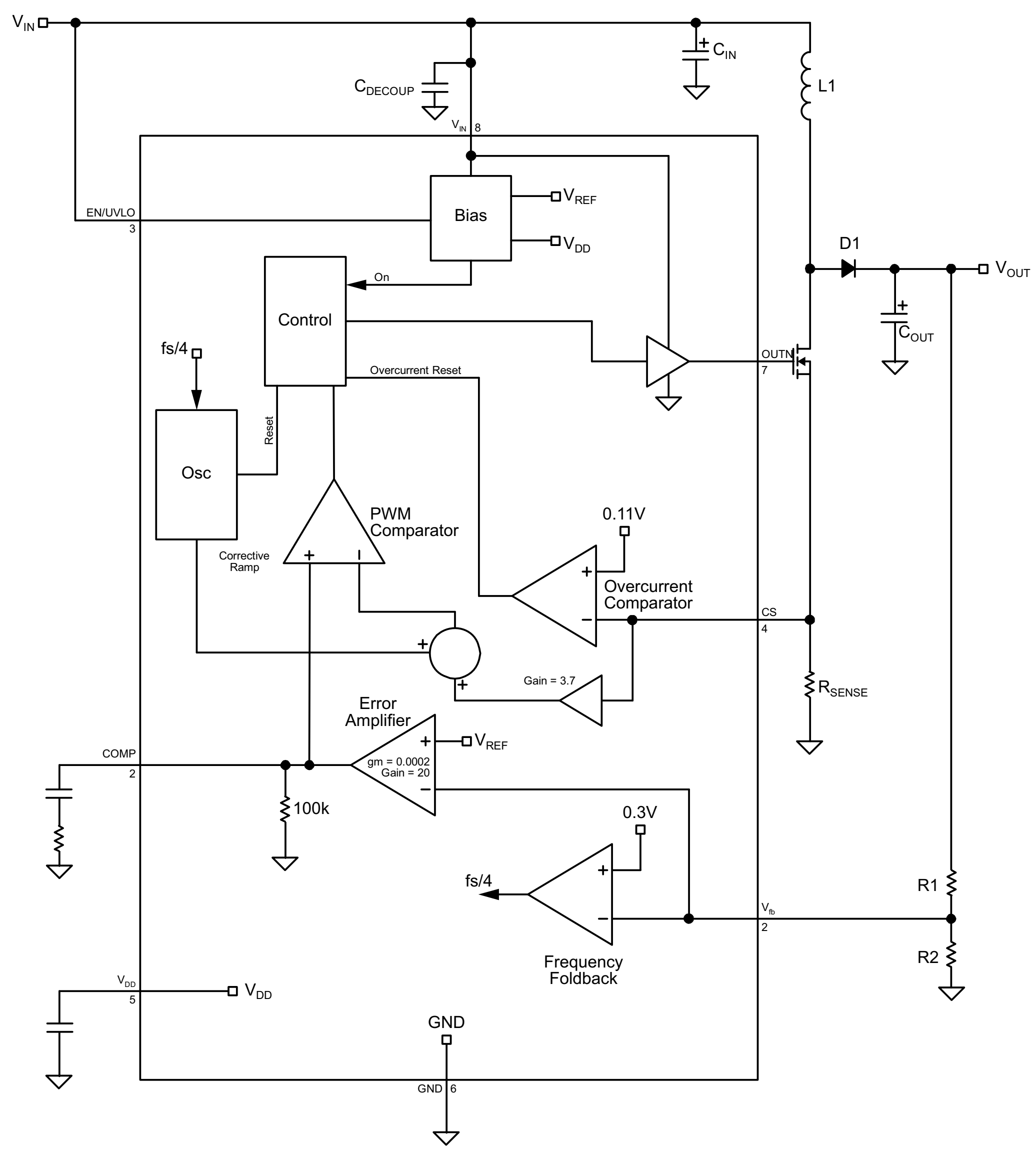


Typical Application Circuit



Adjustable Output Boost Converter

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) .... +15V
Digital Supply Voltage (V_{DD}) .... +7V
Comp Pin Voltage (V_{COMP}) .... –0.3V to +3V
Feedback Pin Voltage (V_{FB}) .... –0.3V to +3V
Enable Pin Voltage ($V_{EN/UVLO}$) .... –0.3V to +15V
Current Sense Voltage (V_{CS}) .... –0.3V to +1V
Power Dissipation (P_D) .... 285 mW @ T_A = +85°C
ESD Rating (Note 1) .... 2 kV

Operating Ratings ‡

Supply Voltage (V_{IN}) .... +2.9V to +14V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Device is ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V; V_{OUT} = 12V; T_A = +25°C. **Bold** values valid for –40°C to +125°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Feedback Voltage Reference	V_{FB}	1.233	1.245	1.258	V	±1%
		1.220	1.245	**1.270**		±2%
Feedback Bias Current	I_{FB}	—	50	—	nA	—
Output Voltage Line Regulation	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	—	0.08	—	%/V	3V ≤ V_{IN} ≤ 9V
Output Voltage Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	–1.2	—	%	0 mV ≤ V_{CS} ≤ 75 mV
Output Voltage Total Regulation	V_{OUT_TR}	1.208	—	1.282	V	3V ≤ V_{IN} ≤ 9V; 0 mV ≤ V_{CS} ≤ 75 mV (±3%)
Input and V_{DD} Supply						
V_{IN} Input Current	I_Q	—	1	2	mA	Excluding external MOSFET gate current
Shutdown Quiescent Current	I_{Q_SD}	—	0.5	5	µA	$V_{EN/UVLO}$ = 0V
Digital Supply Voltage	V_{DD}	2.82	3.0	3.18	V	I_L = 0 mA
Digital Supply Load Regulation	V_{DD_LR}	—	0.1	—	V	I_L = 0 mA to 5 mA
Undervoltage Lockout	UVLO	—	2.65	—	V	V_{DD} upper threshold (turn-on threshold)
UVLO Hysteresis	$UVLO_{HYS}$	—	100	—	mV	—
Enable/UVLO						
Enable Input Threshold	V_{EN_TH}	0.6	0.9	1.2	V	—

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 5V; V_{OUT} = 12V; T_A = +25°C. **Bold** values valid for –40°C to +125°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
UVLO Threshold	$UVLO_{TH}$	1.4	1.5	1.6	V	—
Enable Input Current	I_{EN}	—	0.2	5	µA	$V_{EN/UVLO}$ = 5V
Current Limit						
Current Limit Threshold Voltage	V_{ILIM_TH}	90	110	130	mV	Voltage on CS to trip current limit
Error Amplifier						
Error Amplifier Gain	EA_{GAIN}	—	20	—	V/V	—
Current Amplifier						
Current Amplifier Gain	CA_{GAIN}	—	3.7	—	V/V	—
Oscillator Selection						
Oscillator Frequency	f_O	360	400	440	kHz	—
Maximum Duty Cycle	DC_{MAX}	—	85	—	%	V_{FB} = 1.0V
Minimum On-Time	$t_{ON(MIN)}$	—	165	—	ns	V_{FB} = 1.5V
Frequency Foldback Threshold	V_{FF_TH}	—	0.3	—	V	Measured on FB
Frequency Foldback Frequency	f_{FOLD}	—	90	—	kHz	—
Gate Drivers						
Rise/Fall Time	t_r/t_f	—	25	—	ns	C_L = 3300 pF
Output Driver Impedance	DR_Z	—	2	**6**	Ω	Source, V_{IN} = 12V
		—	2	**6**		Sink, V_{IN} = 12V
		—	3	**7**		Source, V_{IN} = 5V
		—	3	**7**		Sink, V_{IN} = 5V

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Junction Temperature Range	T_J	–40	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance, SOIC 8-Ld	θ_{JA}	—	140	—	°C/W	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

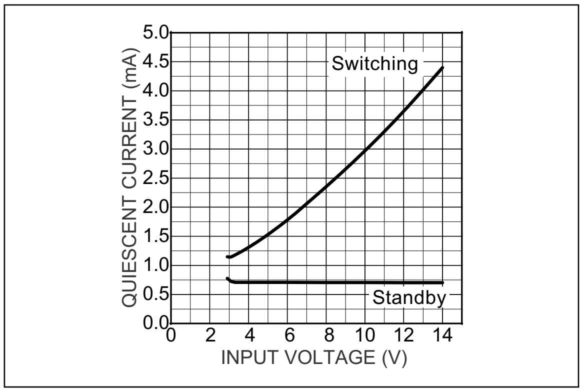


FIGURE 2-1: *Quiescent Current vs. Supply Voltage.*

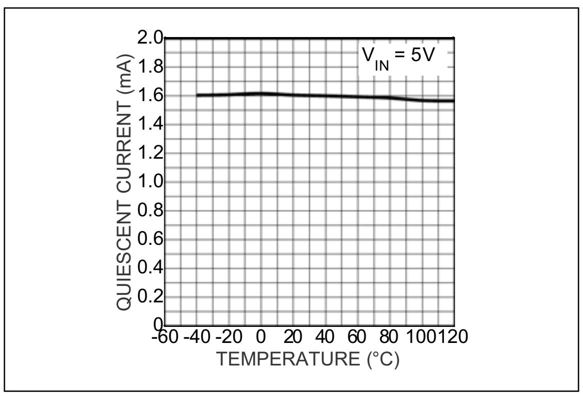


FIGURE 2-2: *Quiescent Current vs. Temperature.*

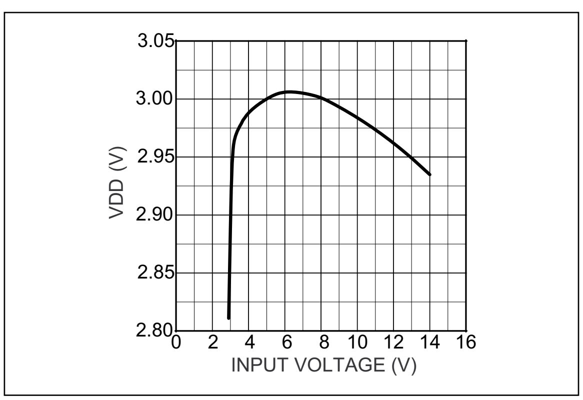


FIGURE 2-3: *V_{DD} vs. Input Voltage.*

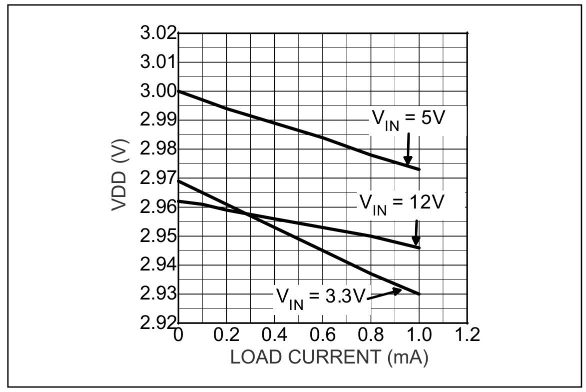


FIGURE 2-4: *V_{DD} vs Load Current.*

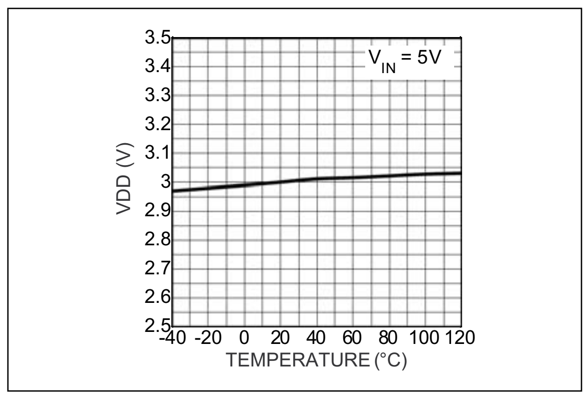


FIGURE 2-5: *V_{DD} vs. Temperature.*

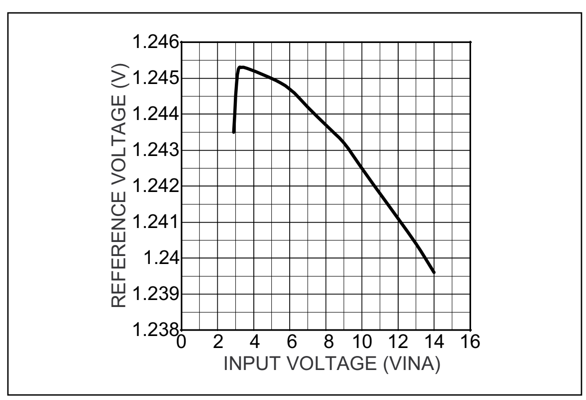


FIGURE 2-6: *Reference Voltage vs. Input Voltage.*

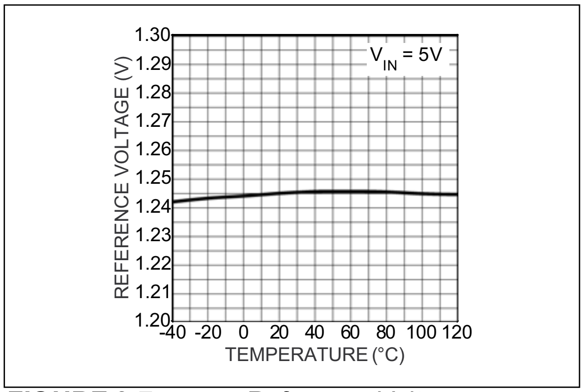


FIGURE 2-7: *Reference Voltage vs. Temperature.*

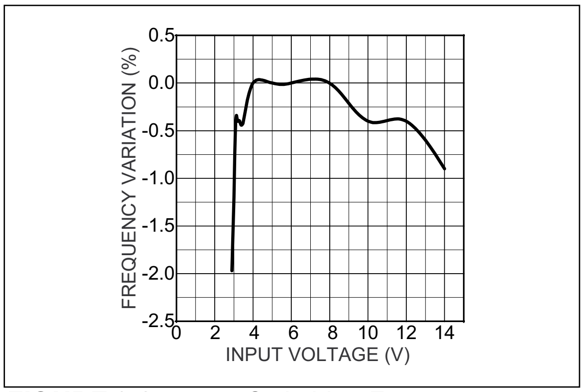


FIGURE 2-8: *Switching Frequency vs. Input Voltage.*

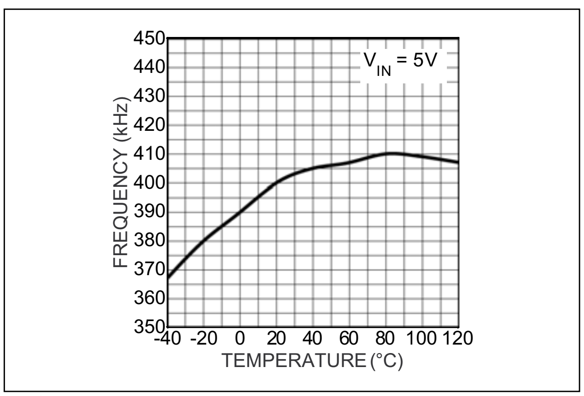


FIGURE 2-9: *Frequency vs. Temperature.*

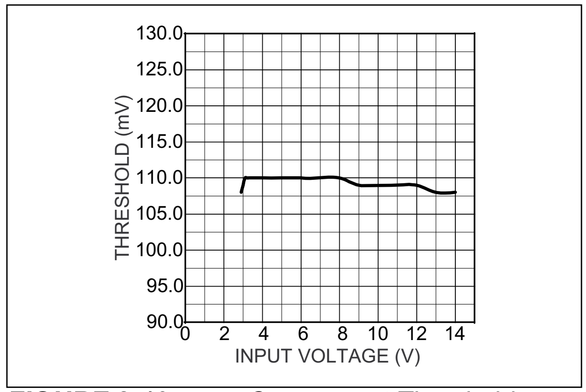


FIGURE 2-10: *Overcurrent Threshold vs. Input Voltage.*

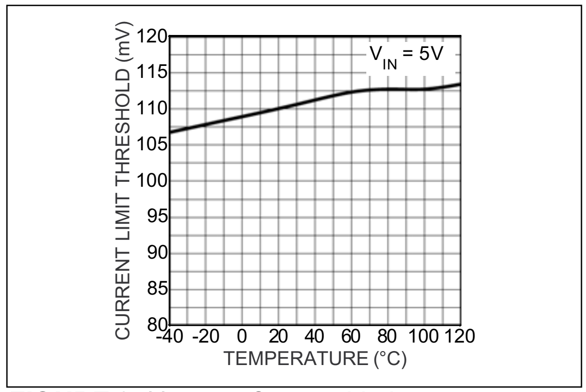


FIGURE 2-11: *Current Limit vs. Temperature.*

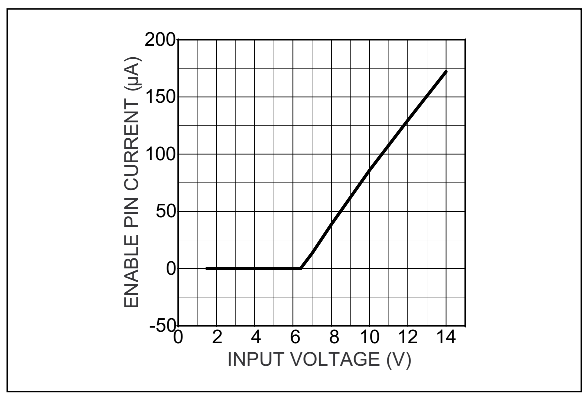


FIGURE 2-12: *Enable Pin vs. Input Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	COMP	Compensation (Output): Internal error amplifier output. Connect to a capacitor or series RC network to compensate the regulator's control loop.
2	FB	Feedback (Input): Regulates FB to 1.245V.
3	EN/UVLO	Enable/Undervoltage Lockout (input): A low level on this pin will power down the device, reducing the quiescent current to under 0.5 µA. This pin has two separate thresholds, below 1.5V the output switching is disabled, and below 0.9V the device is forced into a complete micropower shutdown. The 1.5V threshold functions as an accurate undervoltage lockout (UVLO) with 100 mV hysteresis.
4	CS	The (+) input to the current limit comparator. A built in offset of 100 mV between CS and GND in conjunction with the current sense resistor sets the current limit threshold level. This is also the (+) input to the current amplifier.
5	VDD	3V internal linear regulator output. VDD is also the supply voltage bus for the chip. Bypass to GND with 1 µF.
6	GND	Ground.
7	OUTN	High current drive for N-Channel MOSFET. Voltage swing is from ground to VIN. R_{ON} is typically 3Ω @ $5V_{IN}$.
8	VIN	Input voltage to the control IC. This pin also supplies power to the gate drive circuit.

4.0 FUNCTIONAL DESCRIPTION

The MIC2196 is a BiCMOS, switched-mode multi-topology controller. It will operate most low-side drive topologies including boost, SEPIC, flyback, and forward. The controller has a low impedance driver capable of switching large N-Channel MOSFETs. It features multiple frequency and duty cycle settings. Current mode control is used to achieve superior transient line and load regulation. An internal corrective ramp provides slope compensation for stable operation above a 50% duty cycle. The controller is optimized for high efficiency, high-performance DC-DC converter applications. The Functional Block Diagram shows a the MIC2196 configured as a PWM boost converter.

The switching cycle starts when OUTN goes high and turns on the low-side, N-Channel MOSFET, Q1. The V_{GS} of the MOSFET is equal to V_{IN}. This forces current to ramp up in the inductor. The inductor current flows through the current sense resistor, R_{SENSE}. The voltage across the resistor is amplified and combined with an internal ramp for stability. This signal is compared with the error voltage signal from the error amplifier. When the current signal equals the error voltage signal, the low-side MOSFET is turned off. The inductor current then flows through the diode, D1, to the output. The MOSFET remains off until the beginning of the next switching cycle.

The description of the MIC2196 controller is broken down into several functions:

- Control Loop
- PWM Operation
- Current Limit
- MOSFET gate drive
- Reference, Enable, and UVLO
- Oscillator

4.1 Control Loop

The MIC2196 operates in PWM (pulse-width modulated) mode.

4.2 PWM Operation

Figure 4-1 shows typical waveforms for PWM mode of operation. The gate drive signal turns on the external MOSFET, which allows the inductor current to ramp up. When the MOSFET turns off, the inductor forces the MOSFET drain voltage to rise until the boost diode turns on and the voltage is clamped at approximately the output voltage.

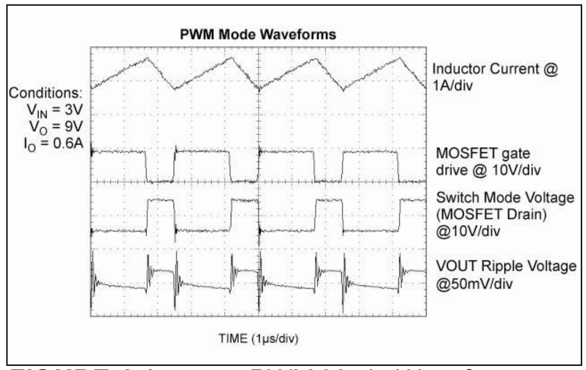


FIGURE 4-1: *PWM Mode Waveforms.*

The MIC2196 uses current mode control to improve output regulation and simplify compensation of the control loop. Current mode control senses both the output voltage (outer loop) and the inductor current (inner loop). It uses the inductor current and output voltage to determine the duty cycle (D) of the buck converter. Sampling the inductor current effectively removes the inductor from the control loop, which simplifies compensation. A simplified current mode control diagram is shown in Figure 4-2.

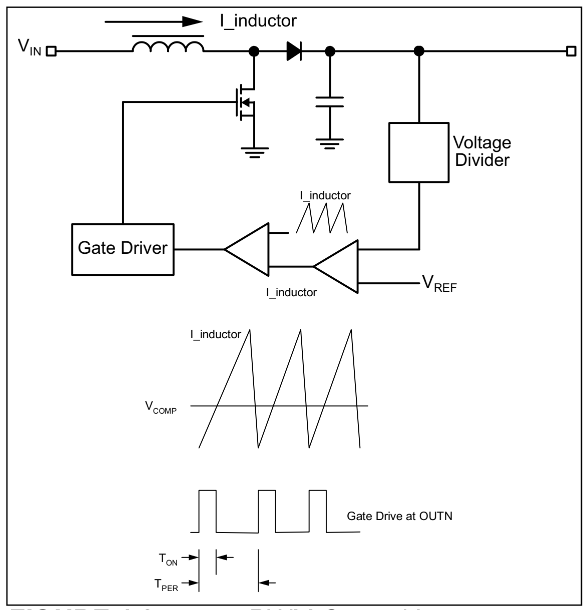


FIGURE 4-2: *PWM Control Loop.*

A diagram of the MIC2196 PWM current mode control loop is shown in the Functional Block Diagram. The inductor current is sensed by measuring the voltage across a resistor, R_{SENSE}. The current sense amplifier buffers and amplifies this signal. A ramp is added to this signal to provide slope compensation, which is required in current mode control to prevent unstable operation at duty cycles greater than 50%.

A transconductance amplifier is used as an error amplifier, which compares an attenuated output voltage with a reference voltage. The output of the error amplifier is compared to the current sense waveform in the PWM block. When the current signal rises above the error voltage, the comparator turns off the low-side drive. The error signal is brought out to the COMP pin (Pin 1) to provide access to the output of the error amplifier. This allows the use of external components to stabilize the voltage loop.

4.3 Current Sensing and Overcurrent Protection

The inductor current is sensed during the switch on time by a current sense resistor located between the source of the MOSFET and ground (R_{SENSE} in the Functional Block Diagram). Exceeding the current limit threshold will immediately terminate the gate drive of the N-Channel MOSFET, Q1. This forces the Q1 to operate at a reduced duty cycle, which lowers the output voltage. In a boost converter, the overcurrent limit will not protect the power supply or load during a severe overcurrent condition or short circuit condition. If the output is short-circuited to ground, current will flow from the input, through the inductor and output diode to ground. Only the impedance of the source and components limits the current.

The mode of operation (continuous or discontinuous), the minimum input voltage, maximum output power and the minimum value of the current limit threshold determine the value of the current sense resistor. Discontinuous mode is where all the energy in the inductor is delivered to the output at each switching cycle. Continuous mode of operation occurs when current always flows in the inductor, during both the low-side MOSFET on and off times. The equations below will help to determine the current sense resistor value for each operating mode.

The critical value of output current in a boost converter is calculated below. The operating mode is discontinuous if the output current is below this value and is continuous if above this value.

EQUATION 4-1:

$$I_{CRIT} = \frac{V_{IN}^2 \times (V_O - V_{IN}) \times \eta}{2 \times f_{SW} \times L \times V_O^2}$$

Where:
η = The efficiency of the boost converter
V_{IN} = The minimum input voltage
L = The value of the boost inductor
f_{SW} = The switching frequency
V_O = The output voltage

4.3.1 MAXIMUM PEAK CURRENT IN DISCONTINUOUS MODE

The peak inductor current is:

EQUATION 4-2:

$$I_{IND(PK)} = \sqrt{\frac{2 \times I_O \times (V_O - \eta \times V_{IN})}{L \times f_{SW}}}$$

Where:
I_O = The maximum output current
V_O = The output voltage
V_{IN} = The minimum input voltage
L = The value of the boost inductor
f_{SW} = The switching frequency
η = The efficiency of the boost converter

The maximum value of current sense resistor is:

EQUATION 4-3:

$$R_{SENSE} = \frac{V_{SENSE}}{I_{IND(PK)}}$$

Where:
V_{SENSE} = The minimum current sense threshold of the CS pin

4.3.2 MAXIMUM PEAK CURRENT IN CONTINUOUS MODE

The peak inductor current is equal to the average inductor current plus one-half of the peak-to-peak inductor current.

The peak inductor current is:

EQUATION 4-4:

$$I_{IND(PK)} = I_{IND(AVE)} + \frac{1}{2} \times I_{IND(PP)}$$

$$I_{IND(PK)} = \frac{V_O \times I_O}{V_{IN} \times \eta} + \frac{V_L \times (V_O - V_{IN} \times \eta)}{2 \times V_O \times f_{SW} \times L}$$

Where:
I_O = The maximum output current
V_O = The output voltage
V_{IN} = The minimum input voltage
L = The value of the boost inductor
f_{SW} = The switching frequency
η = The efficiency of the boost converter
V_L = The voltage across the inductor

V_L may be approximated as V_{IN} for higher input voltage. However, the voltage drop across the inductor winding resistance and low-side MOSFET ON-resistance must be accounted for at the lower input voltages that the MIC2196 operates at:

EQUATION 4-5:

$$V_L = V_{IN} - \frac{V_O \times I_O}{V_{IN} \times \eta} \times (R_{WINDING} + R_{DS(ON)})$$

Where:
$R_{WINDING}$ = The winding resistance of the inductor
$R_{DS(ON)}$ = The ON-resistance of the low-side switching MOSFET

The maximum value of current sense resistor is:

EQUATION 4-6:

$$R_{SENSE} = \frac{V_{SENSE}}{I_{IND(PK)}}$$

Where:
V_{SENSE} = The minimum current sense threshold of the CS pin

The Current Sense pin, CS, is noise sensitive due to the low signal level. The current sense voltage measurement is referenced to the Signal Ground pin of the MIC2196. The current sense resistor ground should be located close to the IC ground. Make sure there are no high currents flowing in this trace. The PCB trace between the high side of the current sense resistor and the CS pin should also be short and routed close to the ground connection. The input to the internal current sense amplifier has a 30 ns dead time at the beginning of each switching cycle. This dead time prevents leading edge current spikes from prematurely terminating the switching cycle. A small RC filter between the Current Sense pin and current sense resistor may help to attenuate larger switching spikes or high frequency switching noise. Adding the filter slows down the current sense signal, which has the effect of slightly raising the overcurrent limit threshold.

4.4 MOSFET Gate Driver

The MIC2196 converter drives a low-side N-Channel MOSFET. The driver for the OUTN pin has a 2Ω typical source and sink impedance. The VIN pin is the supply pin for the gate drive circuit. The maximum supply voltage to the VIN pin is 14V.

4.5 MOSFET Selection

In a boost converter, the V_{DS} of the MOSFET is approximately equal to the output voltage. The maximum V_{DS} rating of the MOSFET must be high enough to allow for ringing and spikes in addition to the output voltage.

The VIN pin supplies the N-Channel gate drive voltage. The V_{GS} threshold voltage of the N-channel MOSFET must be low enough to operate at the minimum V_{IN} voltage to ensure the boost converter will start up.

The maximum amount of MOSFET gate charge that can be driven is limited by the power dissipation in the MIC2196. The power dissipated by the gate drive circuitry is calculated below:

EQUATION 4-7:

$$P\_gate\_drive = Q\_gate \times V_{IN} \times f_{SW}$$

Where:
Q_gate = The total gate charge of the external MOSFET

The graph in Figure 4-3 shows the total gate charge that can be driven by the MIC2196 over the input voltage range. Higher gate charge will slow down the turn-on and turn-off times of the MOSFET, which increases switching losses.

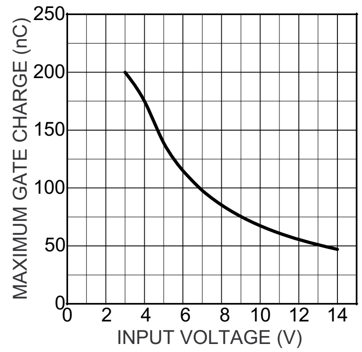


FIGURE 4-3: *MIC2196 Maximum Gate Charge vs. Input Voltage.*

4.6 External Schottky Diode

In a boost converter topology, the boost diode D1, must be rated to handle the peak and average current. The average current through the diode is equal to the average output current of the boost converter. The peak current is calculated in the current limit section of this specification.

For the MIC2196, Schottky diodes are recommended when they can be used. They have a lower forward voltage drop than ultra-fast rectifier diodes, which lowers power dissipation and improves efficiency. They also do not have a recovery time mechanism, which results in less ringing and noise when the diode turns off. If the output voltage of the circuit prevents the use of a Schottky diode, then only ultra-fast recovery diodes should be used. Slower diodes will dissipate more power in both the MOSFET and the diode. The will also cause excessive ringing and noise when the diode turns off.

4.7 Reference, Enable, and UVLO Circuits

The output drivers are enabled when the following conditions are satisfied:

- The V_{DD} voltage (Pin 5) is greater than its undervoltage threshold.
- The voltage on the Enable pin is greater than the enable UVLO threshold.

The internal bias circuitry generates a 1.245V bandgap reference for the voltage error amplifier and a 3V V_{DD} voltage for the internal supply bus. The VDD pin must be decoupled to ground with a 1 µF ceramic capacitor.

The Enable pin (Pin 3) has two threshold levels, allowing the MIC2196 to shut down in a microcurrent mode or turn off output switching in standby mode. Below 0.9V, the device is forced into a micropower shutdown. If the Enable pin is between 0.9V and 1.5V the output gate drive is disabled, but the internal circuitry is powered on and the soft start pin voltage is forced low. There is typically 135 mV of hysteresis below the 1.5V threshold to ensure the part does not oscillate on and off due to ripple voltage on the input. Raising the enable voltage above the UVLO threshold of 1.5V enables the output drivers and allows the soft start capacitor to charge. The enable pin may be pulled up to VINA.

4.8 Oscillator and Sync

The internal oscillator is self-contained and requires no external components. The maximum duty cycle of the MIC2196 is 85%.

Minimum duty cycle becomes important in a boost converter as the input voltage approaches the output voltage. At lower duty cycles, the input voltage can be closer to the output voltage without the output rising out of regulation. Minimum duty cycle is typically 7%.

A frequency foldback mode is enabled if the voltage on the Feedback pin (Pin 2) is less than 0.3V. In frequency foldback the oscillator frequency is reduced by approximately a factor of 4.

4.9 Voltage Setting Components

The MIC2196 requires two resistors to set the output voltage as shown in Figure 4-4.

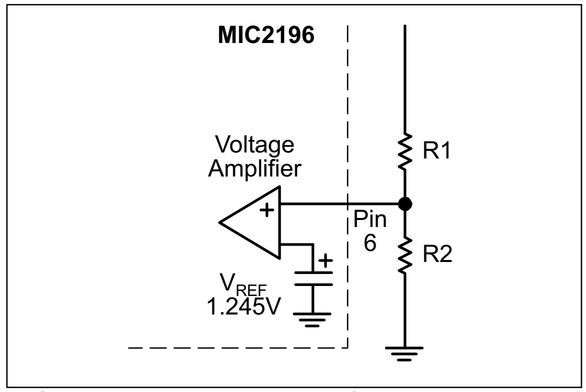


FIGURE 4-4: *Voltage Setting Components.*

The output voltage is determined by the equation below:

EQUATION 4-8:

$$V_O = V_{REF} \times 1 + \frac{R1}{R2}$$

Where:

V_{REF} = 1.245V (nominally) for the MIC2196

Lower values of resistance are preferred to prevent noise from appearing on the VFB pin. A typically recommended value for R1 is 10 kΩ.

4.10 Decoupling Capacitor Selection

A 1 µF decoupling capacitor is used to stabilize the internal regulator and minimize noise on the VDD pin. Placement of this capacitor is critical to the proper operation of the MIC2196. It must be next to the VDD and Signal Ground pins and routed with wide etch. The capacitor should be a good quality ceramic. Incorrect placement of the VDD decoupling capacitor will cause jitter and/or oscillations in the switching waveform as well as variations in the overcurrent limit.

A minimum 1 µF ceramic capacitor is required to decouple the VIN pin. The capacitor should be placed near the IC and connected directly between Pins 8 (VCC) and 6 (GND). For V_{IN} greater than 8V, use a 4.7 µF or a 10 µF ceramic capacitor to decouple the VDD pin.

4.11 Efficiency Calculation and Considerations

Efficiency is the ratio of output power to input power. The difference is dissipated as heat in the boost converter. The significant contributors at light output loads are:

- The VIN pin supply current, which includes the current required to switch the external MOSFETs.
- Core losses in the inductor.

To maximize efficiency at light loads:

- Use a low gate charge MOSFET or use the smallest MOSFET, which is still adequate for the maximum output current.
- Use a ferrite material for the inductor core, which has less core loss than an MPP or iron power core.

The significant contributors to power loss at higher output loads are (in approximate order of magnitude):

- Resistive ON-time losses in the MOSFET
- Switching transition losses in the MOSFET
- Inductor resistive losses
- Current sense resistor losses
- Output capacitor resistive losses (due to the capacitor's ESR)

To minimize power loss under heavy loads:

- Use logic level, low ON-resistance MOSFETs. Multiplying the gate charge by the ON-resistance gives a figure of merit, providing a good balance between switching and resistive power dissipation.
- Slow transition times and oscillations on the voltage and current waveforms dissipate more power during the turn-on and turn-off of the low side MOSFET. A clean layout will minimize parasitic inductance and capacitance in the gate drive and high current paths. This will allow the fastest transition times and waveforms without oscillations. Low gate charge MOSFETs will switch faster than those with higher gate charge specifications.
- For the same size inductor, a lower value will have fewer turns and therefore, lower winding resistance. However, using too small of a value will increase the inductor current and therefore require more output capacitors to filter the output ripple.
- Lowering the current sense resistor value will decrease the power dissipated in the resistor. However, it will also increase the overcurrent limit and may require larger MOSFETs and inductor components to handle the higher currents.
- Use low ESR output capacitors to minimize the power dissipated in the capacitor's ESR.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

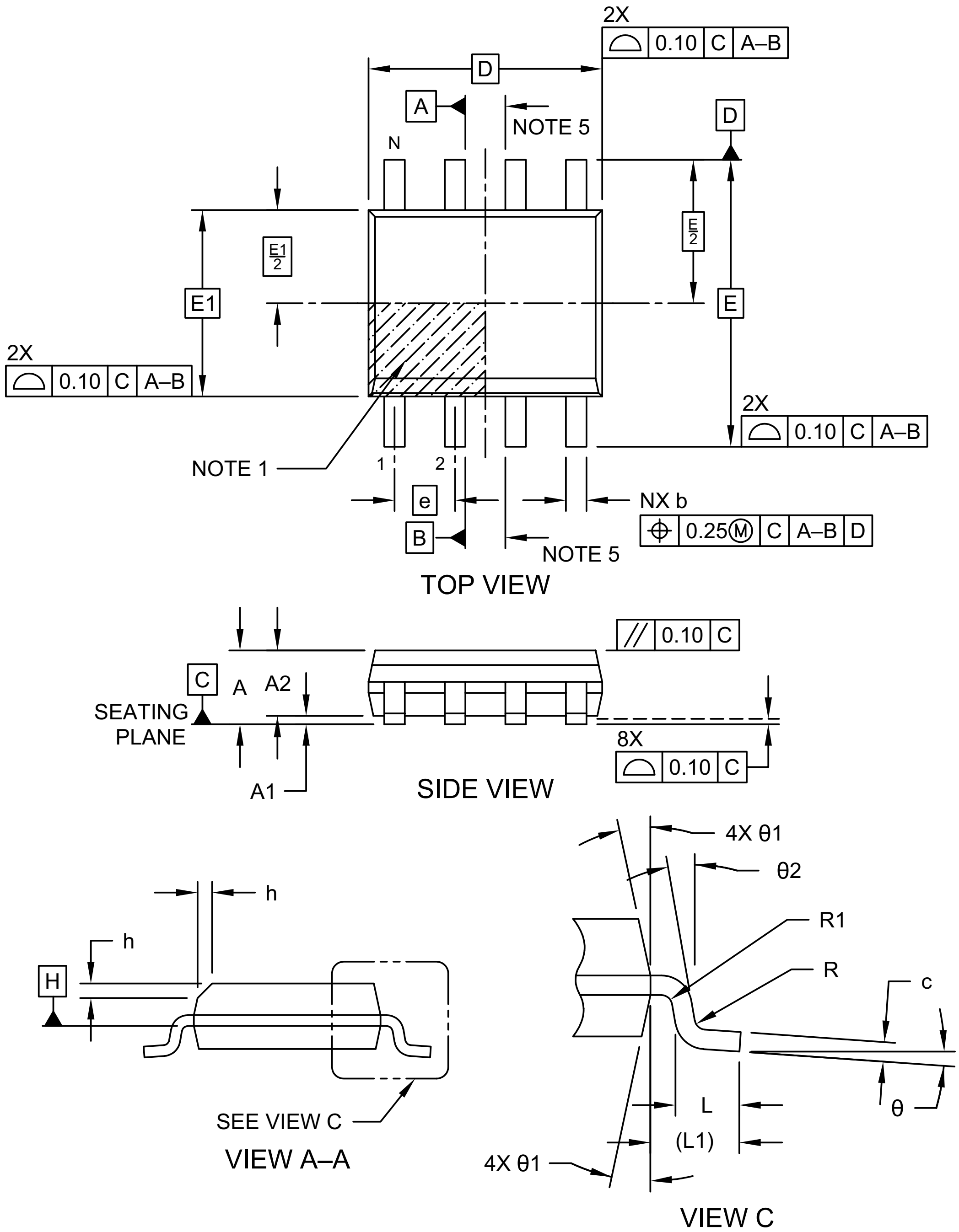
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

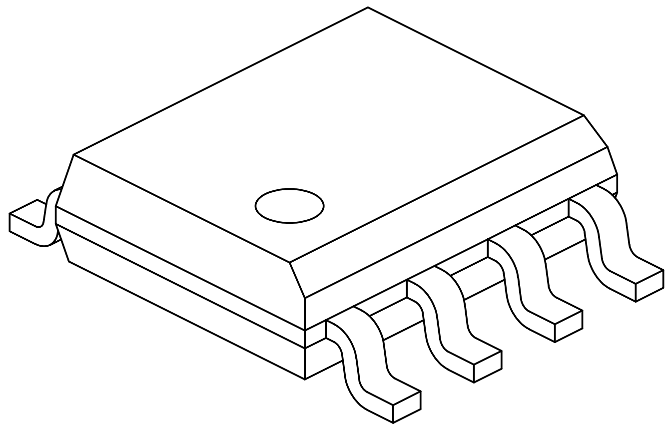
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-3BX Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

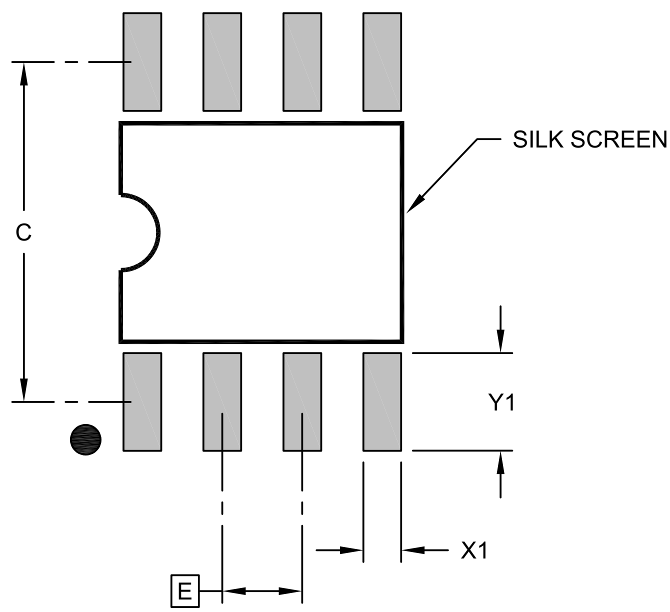
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-3BX Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-3BX Rev K

APPENDIX A: REVISION HISTORY

Revision A (August 2024)

- Converted Micrel document MIC2196 to Microchip data sheet DS20006813A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number	[X]	X	XX	[-XX]
Device	Output Voltage	Temperature Range	Package	Media Type

Device:	MIC2196:		400 kHz SOIC-8 Boost Control IC
Output Voltage:	<blank>	=	Adjustable
Temperature Range:	Y	=	–40°C to +125°C
Package:	M	=	8-Lead SOIC
Media Type:	<blank> TR	= =	95/Tube 2,500/Reel

Examples:

a) MIC2196YM: MIC2196, Adjustable Output Voltage, –40°C to +125°C Temp. Range, 8-Lead SOIC, 95/Tube

b) MIC2196YM-TR: MIC2196, Adjustable Output Voltage, –40°C to +125°C Temp. Range, 8-Lead SOIC, 2,500/Reel

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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