LAN9312

High Performance Two Port 10/100 Managed Ethernet Switch with 32-Bit Non-PCI CPU Interface

PRODUCT FEATURES

Data Brief

Highlights

- High performance and full featured 2 port switch with VLAN, QoS packet prioritization, Rate Limiting, IGMP monitoring and management functions
- Easily interfaces to most 32-bit embedded CPU's
- Unique Virtual PHY feature simplifies software development by mimicking the multiple switch ports as a single port MAC/PHY
- Integrated IEEE 1588 Hardware Time Stamp Unit

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions
- Digital video recorders
- VoIP/Video phone systems
- Home gateways
- Test/Measurement equipment
- Industrial automation systems

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM
  - 1K entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1d spanning tree protocol support
  - QoS/CoS Packet prioritization
    - 4 dynamic QoS queues per port
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable class of service map based on input priority
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress/egress ports with random early discard, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any ports or port pairs
  - Fully compliant statistics (MIB) gathering counters
  - Control registers configurable on-the-fly
- Ports
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - Full and half duplex support
  - Full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding
  - 2K Jumbo packet support
  - Programmable interframe gap, flow control pause value
  - Full transmit/receive statistics
  - Auto-negotiation
  - Automatic MDI/MDI-X
  - Loop-back mode
- High-performance host bus interface
  - Provides in-band network communication path
  - Access to management registers
  - Simple, SRAM-like interface
  - 32-bit data bus
  - Big, little, and mixed endian support
  - Large TX and RX FIFO's for high latency applications
  - Programmable water marks and threshold levels
  - Host interrupt support
- IEEE 1588 Hardware Time Stamp Unit
  - Global 64-bit tunable clock
  - Master or slave mode per port
  - Time stamp on TX or RX of Sync and Delay_req packets per port, Timestamp on GPIO
  - 64-bit timer comparator event generation (GPIO or IRQ)
- Comprehensive Power Management Features
  - Wake on LAN
  - Wake on link status change (energy detect)
  - Magic packet wakeup
  - Wakeup indicator event signal
- Other Features
  - General Purpose Timer
  - Serial EEPROM interface (I^2C master or Microwire™ master) for non-managed configuration
  - Programmable GPIOs/LEDs
- Single 3.3V power supply
- Available in Commercial Temp. Range

Order Numbers:

LAN9312-NU For 128-Pin, VTQFP Lead-Free RoHS Compliant Package (0 TO 70°C Temp Range)

LAN9312-NZW For 128-Pin, XVTQFP Lead-Free RoHS Compliant Package (0 TO 70°C Temp Range)

LAN9312-NU-TR For 128-Pin, VTQFP Lead-Free RoHS Compliant Package (0 TO 70°C Temp Range)

LAN9312-NZW-TR For 128-Pin, XVTQFP Lead-Free RoHS Compliant Package (0 TO 70°C Temp Range)

TR indicates tape & reel option.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

General Description

The LAN9312 is a full featured, 2 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9312 combines all the functions of a 10/100 switch system, including the switch fabric, packet buffers, buffer manager, media access controllers (MACs), PHY transceivers, and host bus interface. The LAN9312 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol specification and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

At the core of the LAN9312 is the high performance, high efficiency 3 port Ethernet switch fabric. The switch fabric contains a 3 port VLAN layer 2 switch engine that supports untagged, VLAN tagged, and priority tagged frames. The switch fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 1K entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the buffer manager block within the switch fabric. All aspects of the switch fabric are managed via the switch fabric configuration and status registers, which are indirectly accessible via the memory mapped system control and status registers.

The LAN9312 provides 2 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9312 provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the Host MAC are used to connect the LAN9312 switch fabric to the host bus interface. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. Automatic 32-bit CRC generation/checking and automatic payload padding are supported to further reduce CPU overhead. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while deceasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the LAN9312.

The integrated Host Bus Interface (HBI) easily interfaces to most 32-bit embedded CPU's via a simple SRAM like interface, enabling switch fabric access via the internal Host MAC and allowing full control over the LAN9312 via memory mapped system control and status registers. The HBI supports 32-bit operation with big, little, and mixed endian operations. Four separate FIFO mechanisms (TX/RX Data FIFO's, TX/RX Status FIFO's) interface the HBI to the Host MAC and facilitate the transferring of packet data and status information between the host CPU and the switch fabric. The LAN9312 also provides power management features which allow for wake on LAN, wake on link status change (energy detect), and magic packet wakeup detection. A configurable host interrupt pin allows the device to inform the host CPU of any internal interrupts.

The LAN9312 contains an I^2C/Microwire master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the LAN9312 at reset.

In addition to the primary functionality described above, the LAN9312 provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, a 12-bit configurable GPIO/LED interface, and IEEE 1588 time stamping on all ports and select GPIOs. The IEEE time stamp unit provides a 64-bit tunable clock for accurate PTP timing and a timer comparator to allow time based interrupt generation.

The LAN9312's performance, features and small size make it an ideal solution for many applications in the consumer electronics and industrial automation markets. Targeted applications include: set top boxes (cable, satellite and IP), digital televisions, digital video recorders, voice over IP and video phone systems, home gateways, and test and measurement equipment. System-level and block-level diagrams of the LAN9312 can be seen in on the following pages.

System Level Block Diagram

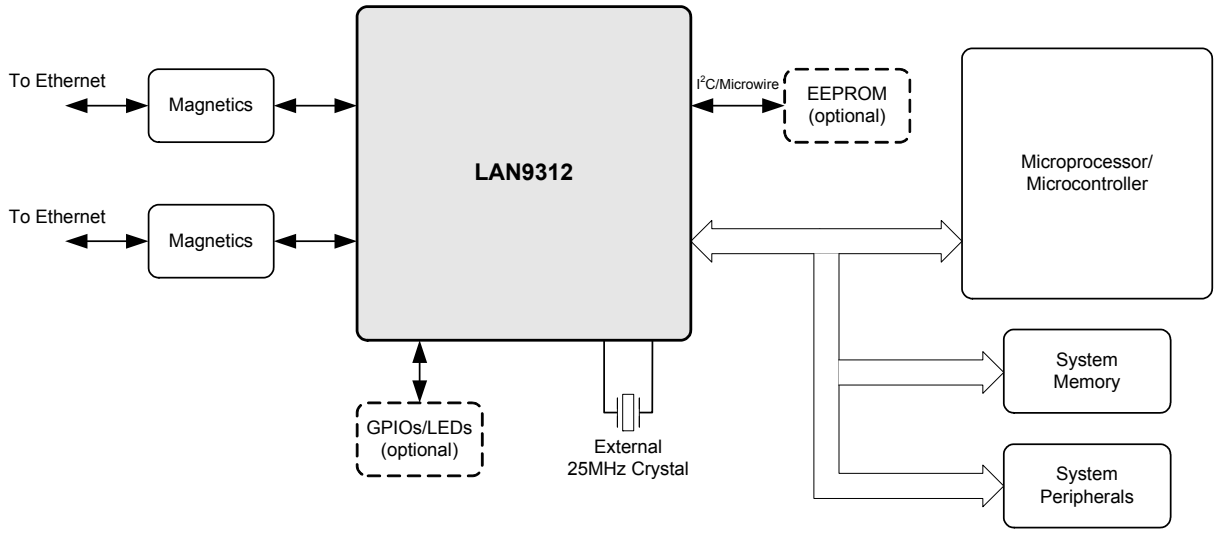

Figure 1 System Level Block Diagram Utilizing the LAN9312

Internal Block Diagram

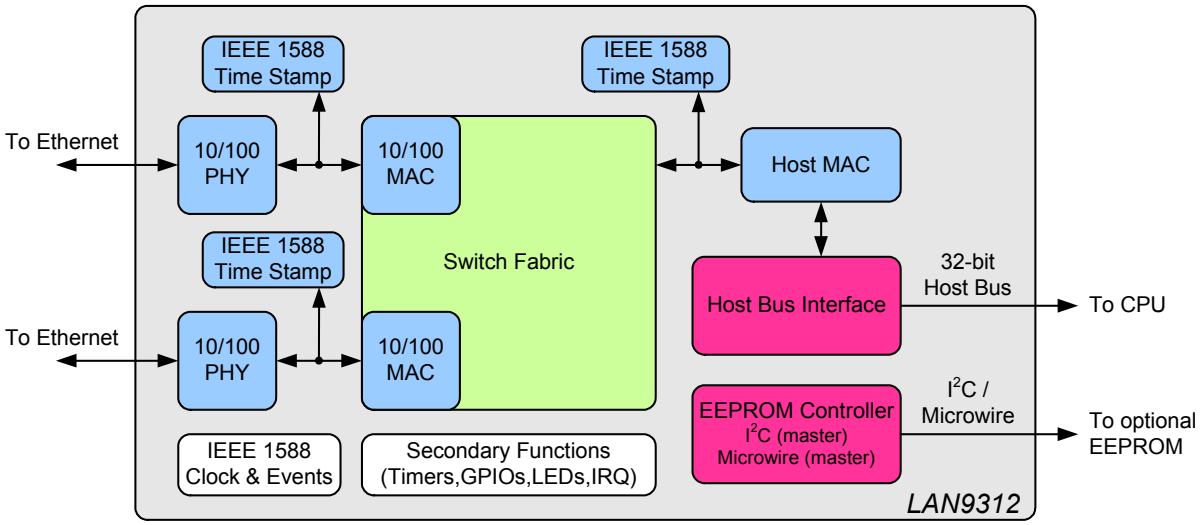

Figure 2 LAN9312 Internal Block Diagram

128-VTQFP Package Outline

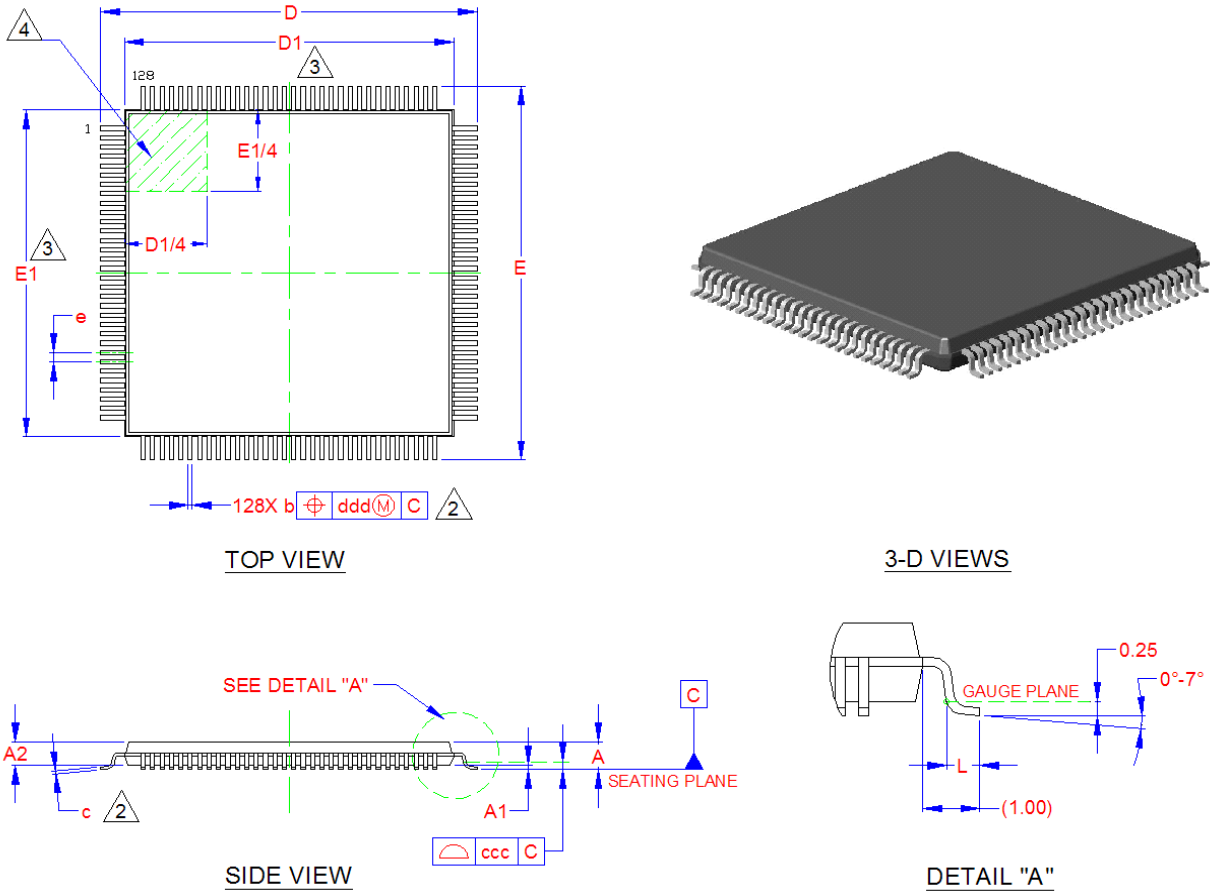

Figure 3 LAN9312 128-VTQFP Package Definition

Table 1 LAN9312 128-VTQFP Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	-	-	1.20	Overall Package Height
A1	0.05	-	0.15	Standoff
A2	0.95	1.00	1.05	Body Thickness
D/E	15.80	16.00	16.20	X/Y Span
D1/E1	13.80	14.00	14.20	X/Y Plastic Body Size
L	0.45	0.60	0.75	Lead Foot Length
b	0.13	0.18	0.23	Lead Width
c	0.09	-	0.20	Lead Foot Thickness
e	0.40 BSC			Lead Pitch
ddd	0.00	-	0.07	True Position Spread
ccc	-	-	0.08	Coplanarity

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimensions b & c apply to the flat section of the lead foot between 0.10 and 0.25mm from the lead tip. The base metal is exposed at the lead tip.
3. Dimensions D1 and E1 do not include mold protrusions. Maximum allowed protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. The pin 1 identifier may vary, but is always located within the zone indicated.

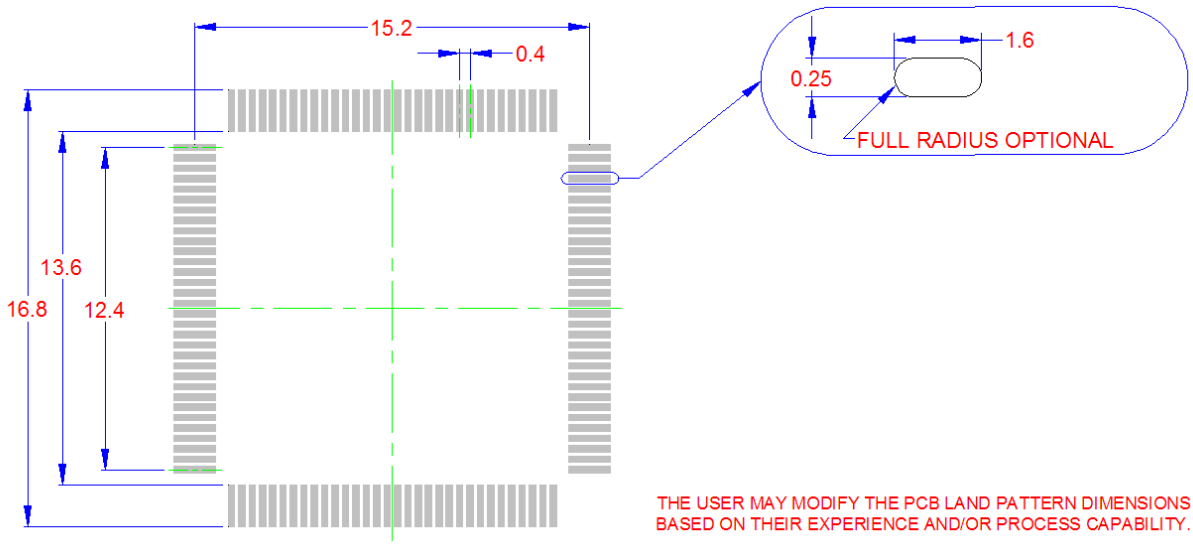

Figure 4 LAN9312 128-VTQFP Recommended PCB Land Pattern

128-XVTQFP Package Outline

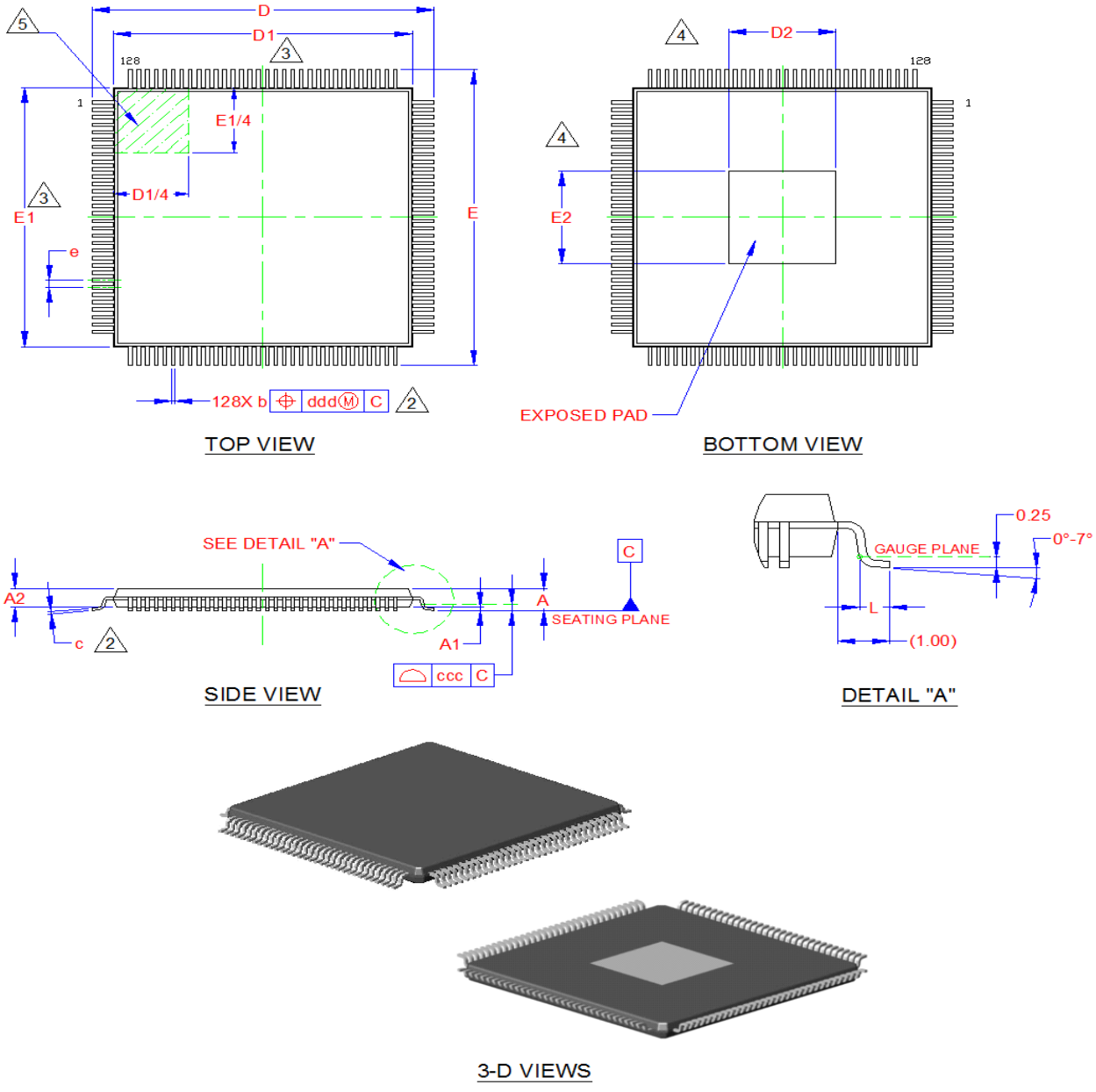

Figure 5 LAN9312 128-XVTQFP Package Definition

Table 2 LAN9312 128-XVTQFP Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	-	-	1.20	Overall Package Height
A1	0.05	-	0.15	Standoff
A2	0.95	1.00	1.05	Body Thickness
D/E	15.80	16.00	16.20	X/Y Span
D1/E1	13.80	14.00	14.20	X/Y Plastic Body Size
D2/E2	6.35	6.50	6.65	X/Y Exposed Pad Size
L	0.45	0.60	0.75	Lead Foot Length
b	0.13	0.18	0.23	Lead Width
c	0.09	-	0.20	Lead Foot Thickness
e		0.40 BSC		Lead Pitch
ddd	0.00	-	0.07	True Position Spread
ccc	-	-	0.08	Coplanarity

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimensions b & c apply to the flat section of the lead foot between 0.10 and 0.25mm from the lead tip. The base metal is exposed at the lead tip.
3. Dimensions D1 and E1 do not include mold protrusions. Maximum allowed protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimensions D2 and E2 represent the size of the exposed pad. The exposed pad shall be coplanar with the bottom of the package within 0.05mm.
5. The pin 1 identifier may vary, but is always located within the zone indicated.

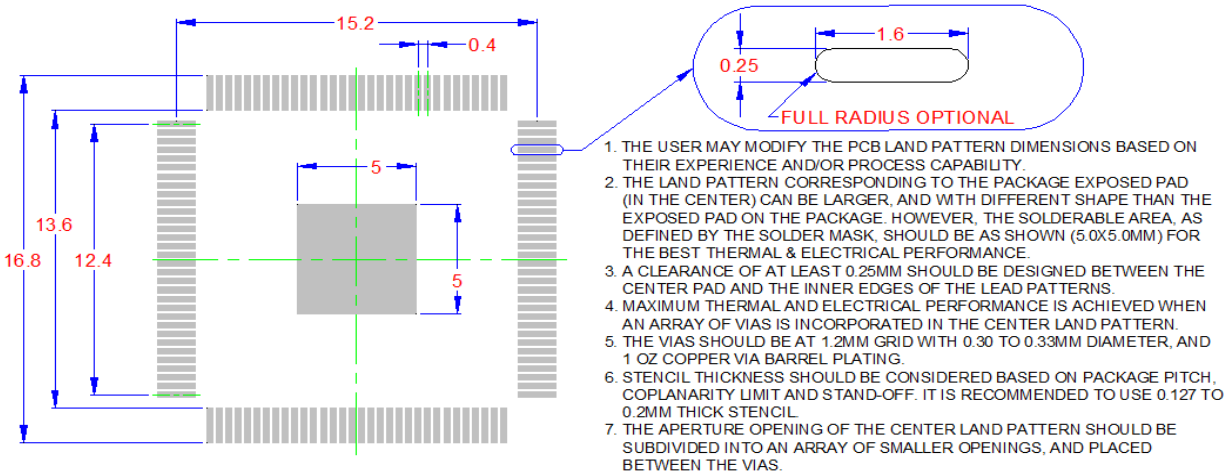

Figure 6 LAN9312 128-XVTQFP Recommended PCB Land Pattern