合力为科技
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HLW8110/HLW8112 DataSheet
REV 1.01

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MeterIC

DataSheet **HLW8110/HLW8112**

1 Application

- Intelligent household appliances
- Leakage Detection Equipment
- Metering Meter
- Metering Plug
- Wifi Plug
- Charging pile
- PDU
- LED
- Traffic lights

2 REVISION HISTORY

Data	Changes	Revision
2019-09-12	Initial version	REV 1.00
2020-11-20	Update Schematic	REV 1.01

目录

3 FEATURES

- ✓ Instantaneous Voltage, Current, and Power
- ✓ Leakage detection、Power Factor, and Line Frequency
- ✓ Less than 0.1% error in active energy measurements over a dynamic range of 5000:1
- ✓ Less than 0.1% error in instantaneous Active Power measurement over a dynamic range of 3000:1
- ✓ Less than 0.1% error in instantaneous VRMS measurement over a dynamic range of 1000:1
- ✓ Less than 0.1% error in instantaneous IRMS measurement over a dynamic range of 1000:1
- ✓ Active power overload indication
- ✓ Zero-crossing detection、Overvoltage indication, undervoltage indication
- ✓ Internal Frequency Oscillator
- ✓ Working Voltage Support 3.3V and 5.0V
- ✓ SPI/UART
- ✓ SOP8/SSOP16

4 Description

HLW8110/HLW8112 is a high precision power metering IC. It can measure line voltage and current, and calculate active power. It can measure Line Frequency and Power Factor.

HLW8110/HLW8112 has three detection channels, including current detection channels A and B, and voltage detection channels.

A channel and B channel can be used for current detection at the same time.

B-channel can be used for current detection or leakage detection.

HLW8112 contains two configurable pulse output pins, which can be used to acquire over-current, over-voltage, zero-crossing voltage or current detection and leakage detection through INT1 and INT2 pins.

HLW8110/HLW8112 power metering IC uses 3.3V or 5.0V power supply with Internal Frequency Oscillator.

5 Function block diagram

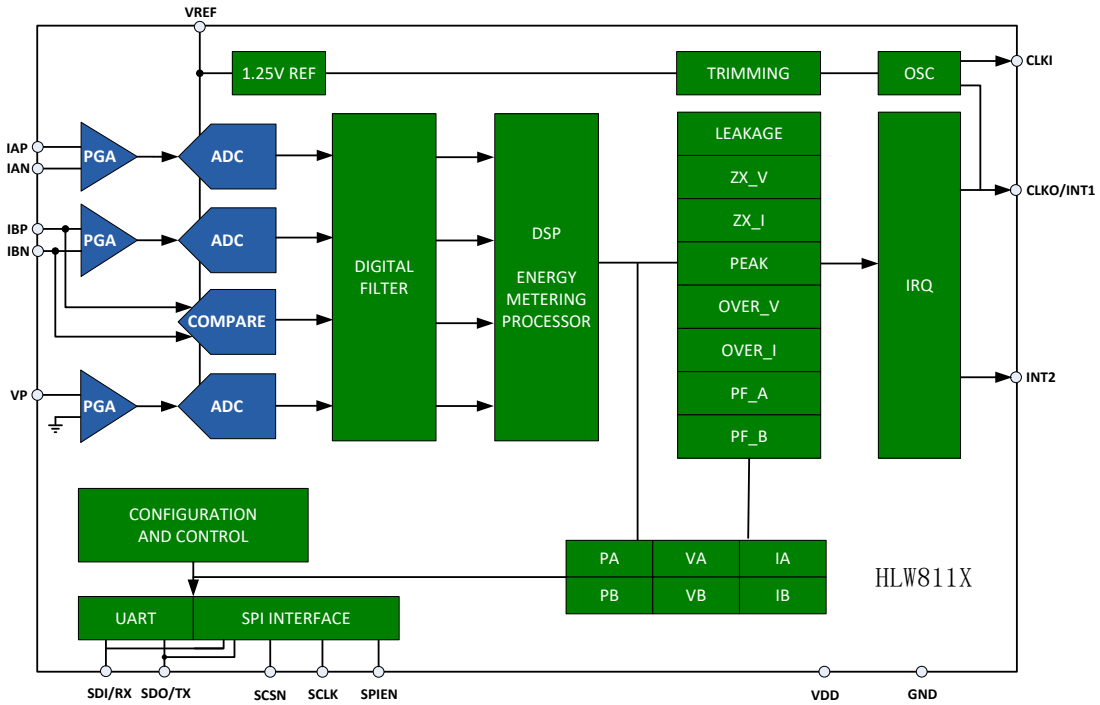


Figure 1 Function block diagram

6 PIN DESCRIPTION

6.1 HLW8110 Pin Configuration

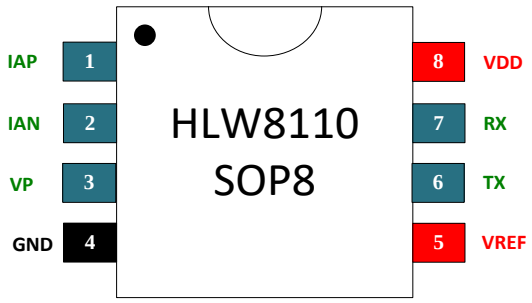


Figure 2 HLW8110 Pin Configuration

Table 1 HLW8110 pin function description

PIN NO.	PIN Name	Input/Output	Description
1	IAP	Input	Differential analog input pins for the current channel A,The maximum input range of the differential voltage is peak value (+800mV/PGA)
2	IAN	Input	Differential analog input pins for the current channel A,The maximum input range of the differential voltage is peak value (+800mV/PGA)
3	VP	Input	Differential analog input pins for the voltage channel,the maximum input range of the voltage is peak value (+800mV/PGA).
4	GND	Ground	Analog ground
5	VREF	Input/Output	The pin can use on-chip reference voltage, which is parallel to 0.1uF decoupling capacitor.
6	TX	Output	UART Tx Data
7	RX	Input	UART Rx Data
8	VDD	Power Supply	VDD Power Supply VDD 1:3.0-3.6V. Suggest 3.3V. VDD 2:4.5V-5.5V, Suggest 5.0V.

6.2 HLW8110 typical application

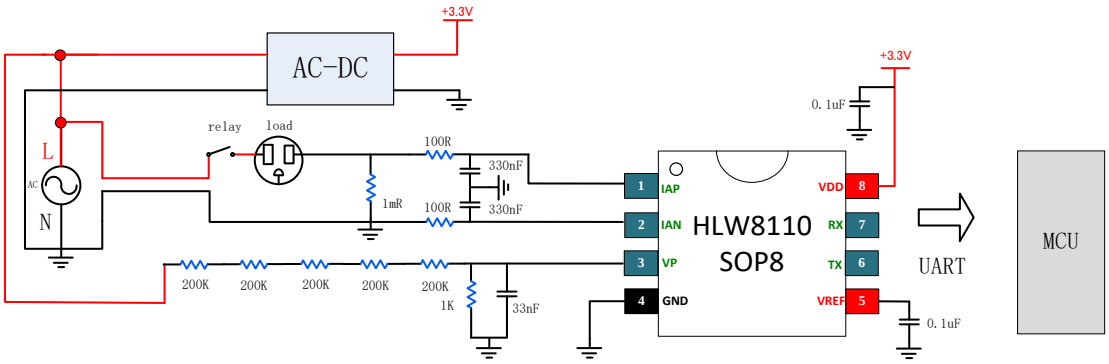


Figure 3 HLW8110 typical application

6.3 HLW8112 Pin Configuration

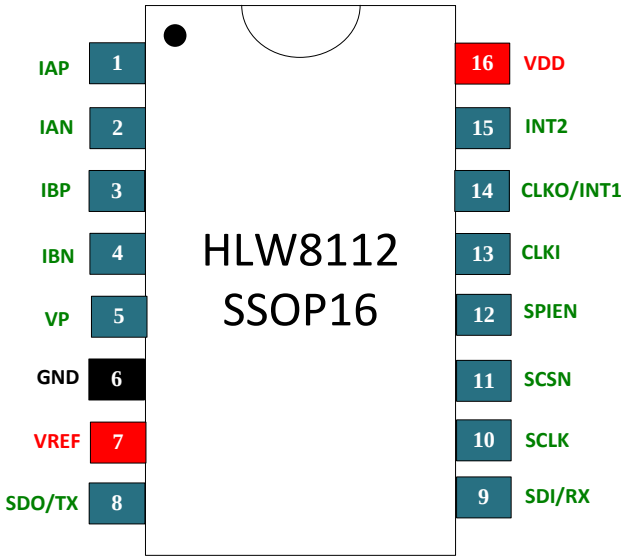


Figure 4 HLW8112 Pin Configuration

Table 2 HLW8112 pin function description

PIN NO.	PIN Name	Input/Output	Description

1	IAP	Input	Differential analog input pins for the current channel A,The maximum input range of the differential voltage is peak value (+800mV/PGA)
2	IAN	Input	Differential analog input pins for the current channel A,The maximum input range of the differential voltage is peak value (+800mV/PGA)
3	IBP	Input	Differential analog input pins for the current channel B,The maximum input range of the differential voltage is peak value (+800mV/PGA)
4	IBN	Input	Differential analog input pins for the current channel B,The maximum input range of the differential voltage is peak value (+800mV/PGA)
5	VP	Input	Differential analog input pins for the voltage channel,the maximum input range of the voltage is peak value (+800mV/PGA).
6	GND	Ground	Analog ground
7	REF	Input	The pin can use on-chip reference voltage, which is parallel to 0.1uF decoupling capacitor.
8	SDO/TX	Output	1、 Serial port data output pin 2、 UART TX Data
9	SDI/RX	Input	1、 Serial port data input pin 2、 UART Tx Data
10	SCLK	Input	SPI Communication mode：SPI CLOCK UART Communication mode： Configuration baud rate
11	SCSN	Input	SPIEN = 0，UART Communication mode： Configuration baud rate SPIEN = 1，SPI Communication mode： 1、SCSN = 0，SPI is effective； 2、SCSN = 1，SPI is invalid；
12	SPIEN	Input	SPIEN = 0，UART Communication mode； SPIEN = 1，SPI Communication mode；
13	CLKI	Input	External crystal Input port，Recommended 3.579M Crystal CLKI = 0, using built-in oscillator
14	CLKO/INT1	Output	1、External crystal output port 2、indicates that an enabled event has occurred.
15	INT2	Output	indicates that an enabled event has occurred.
16	VDD	Power Supply	VDD Power Supply VDD 1:3.0-3.6V. Suggest 3.3V. VDD 2:4.5V-5.5V, Suggest 5.0V.

6.4 HLW8112 typical application

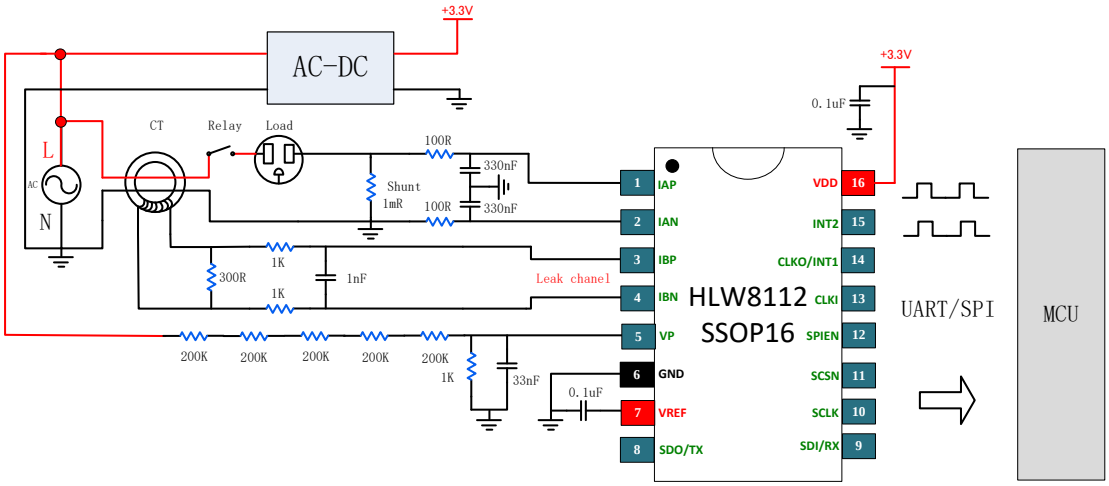


Figure 5 HLW8112 typical application

7 Feature Description

7.1 RECOMMENDED OPERATING CONDITIONS

Table 3 **RECOMMENDED OPERATING CONDITIONS**

Parameter	symbol	Min	Typ	Max	Unit
Power upply	VDD	4.5	5.0	5.5	V
	VDD	3.0	3.3	3.6	V
reference voltage	VREF	1.24	1.25	1.26	V
IDD	B Channel Close		3.7(VDD =3.3V) 4.3(VDD =5.0V)		mA
	B Channel Open		4.7(VDD =3.3V) 5.3(VDD =5.0V)		mA
Operation Temperature Range	TA	-40		+85	℃

7.2 Analog Characteristics

AVDD = DVDD = 5V ± 10% or 3.3V ± 10%;AGND = DGND = 0V;VREF = 1.25V;

MCLK = 3.579545MHz 。

Table 4 Analog Characteristic Table

Parameter	symbol	Min	Typ	Max	Unit
ACCURACY					
dynamic range of 3000:1 Input Range 0.25%~100%	PActive	-0.1	0	0.1	%
dynamic range of 1000:1 Input Range 0.25%~100%	IRms	-0.1	0	0.1	%
dynamic range of 1000:1 Input Range 0.25%~100%	VRms	-0.1	0	0.1	%
Analog Input					
Maximum Signal Levels	IIN	-800/PGA	-	+800/PGA	mV
Input Impedance	EII	70K	12M/PGA		Ω
Reset Voltage					
detection threshold of Power-On Voltage	PMLO	2.8	2.9	2.95	V
detection Threshold of Power-Down Voltage	PMHI	2.5	2.7	2.9	V
Built-In Reference					
Reference Voltage	VREFOUT	1.24	1.25	1.26	V
Temperature Coefficient	TCVREF		5	15	Ppm/℃

7.3 Digital Characteristics

VDD = DVDD = 5V ± 10% or 3.3V ± 10%;AGND = DGND =0V

MCLK = 3.579545MHZ

Table 5 Digital Characteristic Table

Parameter	symbol	Min	Typ	Max	Unit
BUILT-IN CLOCK					
Frequency (Note2)	MCLK	3.507	3.579	3.65	MHZ

Duty(Note3)		30	-	70	%
FILTER					
phase shift range (50HZ)		−2.56°		+2.56°	°
Sampling Rate (DCLK = MCLK/K)		-	MCLK/4	-	Hz
Digital Filter Output Rate	OWR	-	MCLK/512	-	Hz
High-Pass Filter Bandwidth (-3dB)		-	0.543	-	Hz
Input/Output					
Input High Voltage (DVDD =5V)	VIH	0.5VDD	-	-	V
Input Low Voltage(DVDD = 5V)	VIL	-	-	0.8	V
Output High Voltage IoH = 4.2mA(VDD = 5V) IoH = 1.9mA(VDD = 3.3V)	VOH	0.9*VDD	-	-	V
Output Low Voltage IoL = -4.2mA(VDD = 5V) IoL = -1.9mA(VDD = 3.3V)	VOL	 - -	 - -	 0.5 0.5	 V V
Input Leakage	Iin	-10	-	10	uA

Note： 1. using Internal Frequency Oscillator or external clock input, the OSCI frequency must be 3MHZ~5MHZ.

2.If external MCLK is used, the duty cycle must be 45%~55%

3． When the power supply voltage is 5V and the input signal is 3.3V, each IO generates 250uA current.

7.4 ABSOLUTE MAXIMUM RATINGS

Table 6 **ABSOLUTE MAXIMUM Characteristic Table**

Parameter	symbol	Min	Typ	Max	Unit
Power Supply	VDD	-0.3	-	+6.0	V
VDD to GND		-0.3	-	+6.0	V
IAP、IAN、IBP、IBN、VP		-1		+6	V
Analog Input Voltage	VINA	-0.3	-	VDD+0.3	V
DigitalInput Voltage	VIND	-0.3	-	VDD+0.3	V
DigitalOutput Voltage	VOUTD	-0.3	-	VDD+0.3	V
Operating Temperature Range	TA	-40	-	85	℃
Storage Temperature Range	Tstg	-65	-	150	℃

7.5 Reliability

- The ESD design of ESD-analog IO ensures the passage of +1KV signal; the contact voltage of the whole ESD experiment is 8KV, the air voltage is 15KV, and there is no CF pulse output.
- Design of Anti-Group Pulse (EFT) - 6KV without Load, 4KV with Load, No Pulse
- Anti-high frequency electromagnetic field (error variation < 0.5%)
- No CF Pulse Output under Surge Immunity Test (4KV)
- Error Consistency --- At the same test point, the errors before and after several times are less than 0.1%.

8 Functional Description

8.1 RESET

The chip has three global reset modes: up/down reset, low voltage reset and instruction reset.

(1) On-chip reset threshold voltage is 2.9v, power-off reset threshold voltage is 2.7V and hysteresis voltage is 0.2v, as shown in Figure 1.

(2) When the chip receives the reset instruction, it resets immediately, and the reset is completed after the two system clocks.

When any global reset occurs, the register restores to the initial reset value and the external pin level restores to the initial state. The RST in the system state register is the reset flag bit: when the power-on reset or the instruction reset ends, the position 1 is cleared after reading. It can be used for data request of calibration table after reset.

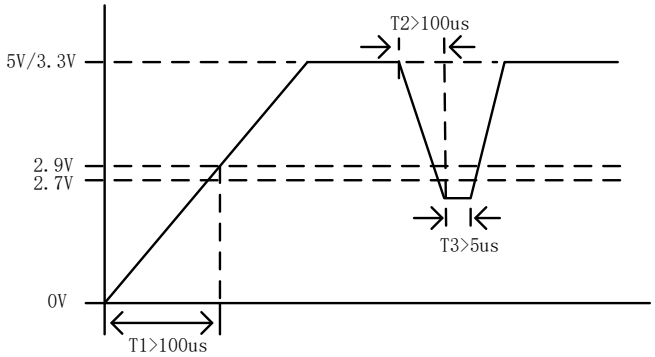


Figure 6 PowrOn and Poweroff Reset Diagram

8.2 Clock Sytem

HLW8112 can use either external crystal oscillator (3.579MHz) or built-in crystal. The CLKI PIN needs to be grounded with built-in oscillator. The typical frequency is 3.579MHz. When using the external crystal, the external capacitor is recommended to use 22pF. The resistance of HLW8112 is connected internally, and the ESR of the external crystal is less than 50 ohms.

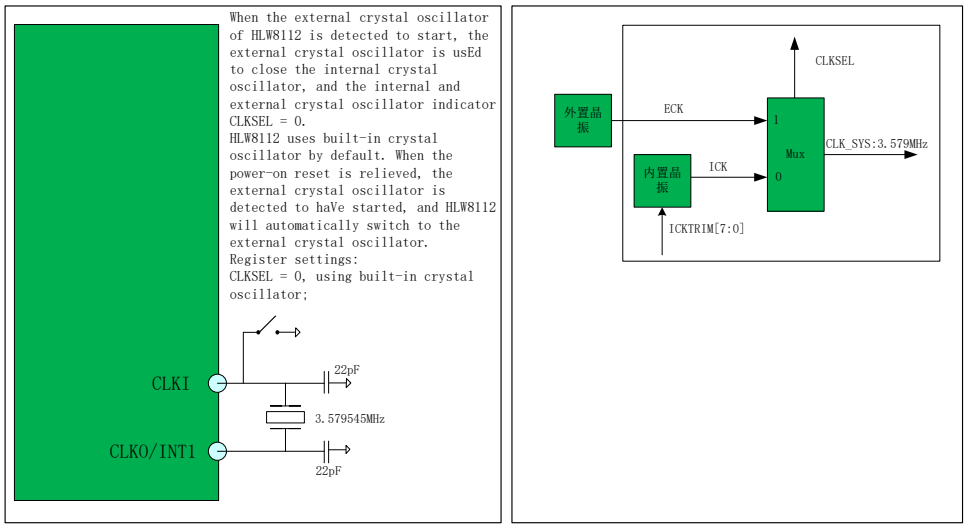


Figure 7 crystal oscillator switching

When the external crystal oscillator of HLW8112 is detected to start, the external crystal oscillator is used to close the internal crystal oscillator, and the internal and external crystal oscillator indicator CLKSEL = 0.

HLW8112 uses built-in crystal oscillator by default. When the power-on reset is relieved, the external crystal oscillator is detected to have started, and HLW8112 will automatically switch to the external crystal oscillator.

Register settings:

CLKSEL = 0, using built-in crystal oscillator;

HLW8110 can only use built-in crystal oscillators

8.3 Analog to Digital Channel

HLW8110/HLW8112 includes three ADC channels, current channels A and B for current sampling, voltage channels for voltage sampling, three ADC channels for full differential input, maximum signal peak value 800mv (PGA = 1).

Table 7 Full range input signals for each channel

PGA	VREF	Full range input (Peak)	PGAIA	PGAIB	PGAIU
1	1.25V	800mV	000	000	000
2		400mV	001	001	001
4		200mV	010	010	010
8		100mV	011	011	011
16		50mV	1XX	1XX	1XX

Note: The RMS of channel effective input signal is peak-to-peak,(800mV/PGA)/$\sqrt{2}$;

8.4 Channel Switching

HLW8110/HLW8112 switches the current channel by special commands to select the current channel of phase angle, apparent power, power factor, instantaneous active power and instantaneous apparent power. The currently selected current channel can be queried through the register bit Channel_sel of EMUStatus.

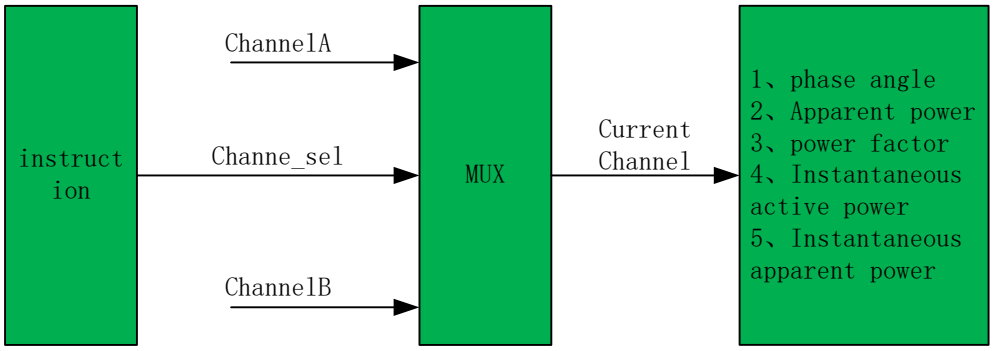


Figure 8 Channel switching diagram

8.5 Active Power

HLW8110/HLW8112 provides two channels of active power calculation and correction, namely, current channel A and voltage channel active power calculation and correction, current channel B and voltage channel active power calculation and correction.

Registers also include A/B two sets of phase correction, active Offset correction, active gain correction, latency determination and average power register.

In addition, in order to ensure the consistency of the two channels, the gain correction register IBGain of current channel B is also provided.

When ADC2ON = 0, the current channel B ADC does not work and the functions related to current channel B do not work.

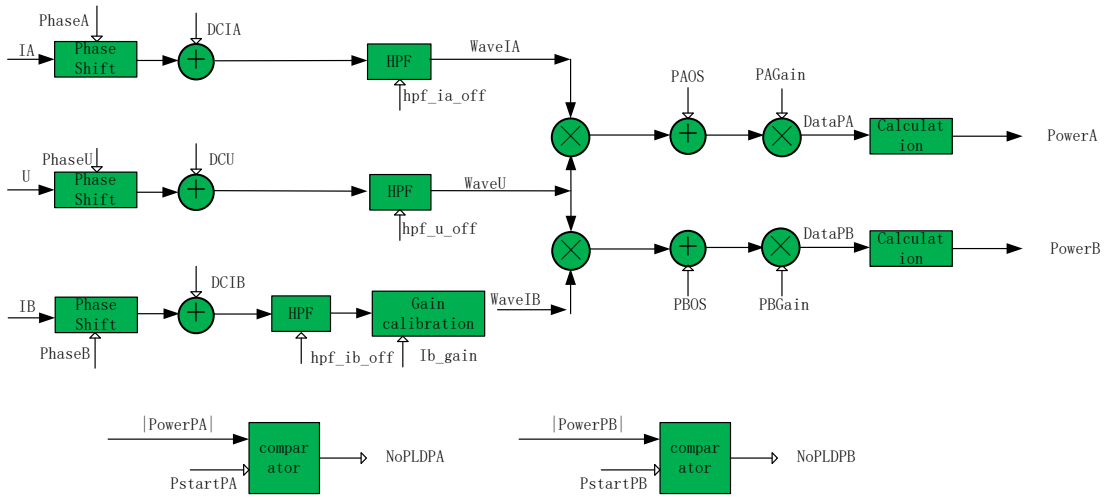


Figure 9 Active power calculation block diagram

8.6 Valid Value

HLW8110/HLW8112 provides three channels of true RMS parameter output, including RmsU, RmsIA and RmsIB. Two RMS Offset registers: RmsIAOS and RmsIBOS.

As shown in the figure below, when DC_MODE=1(close High-pass filter), the operation of RMS will skip the process of self-multiplication, LPF and square, and the waveform data after HPF will directly accumulate and output RMS.

Note: Channel B gain correction (IBGain) will affect the output of RmsIB. Other phase correction, power gain correction and power offset correction will not affect the calculation results of RMS.

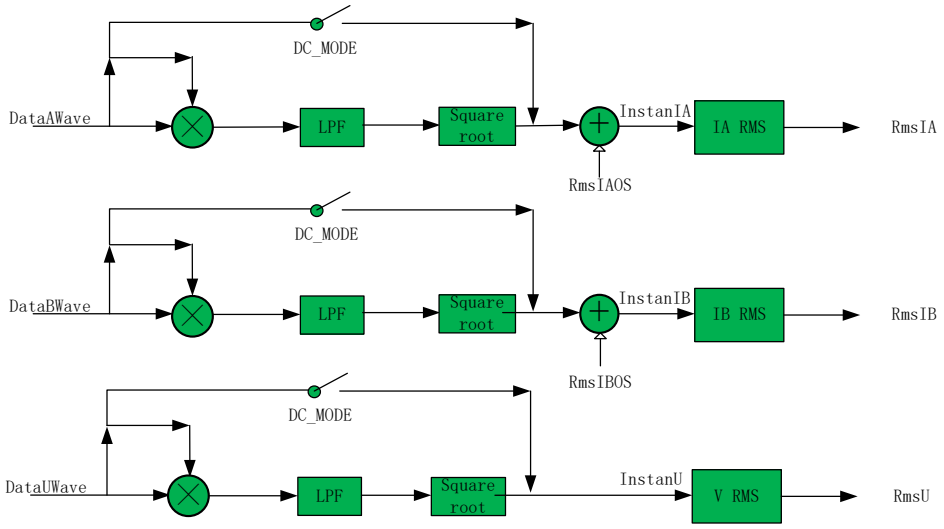


Figure 10 Rms block diagram

8.7 Apparent Power and Power Factor

HLW8110/HLW8112 provides one-way apparent power and power factor (PfactorEN = 1) when calculating power factor: channel A or channel B is selected by command. Optional updating frequencies of power mean register PowerS and power factor register PF are 3.4 Hz, 6.8 Hz, 13.6 Hz and 27.2 Hz.

PowerFactor is a 24-bit signed decimal, the highest bit is the symbol bit, which is obtained by dividing the active power by the apparent power.

Power factor = symbol bit *[(PF22*2^-1)+ (PF21*2^-2)+...] When PF = 7FFFFFH, the power factor is 1.0; when PF = 800000H, the power factor is - 1.0; when PF = 400000H, the power factor is 0.5; when PF = 400000H, the power factor is 7FFFFFH in the latent state;

Users can configure channel selections through special commands, and the results of configurations can be queried through the Channel_sel register bit.

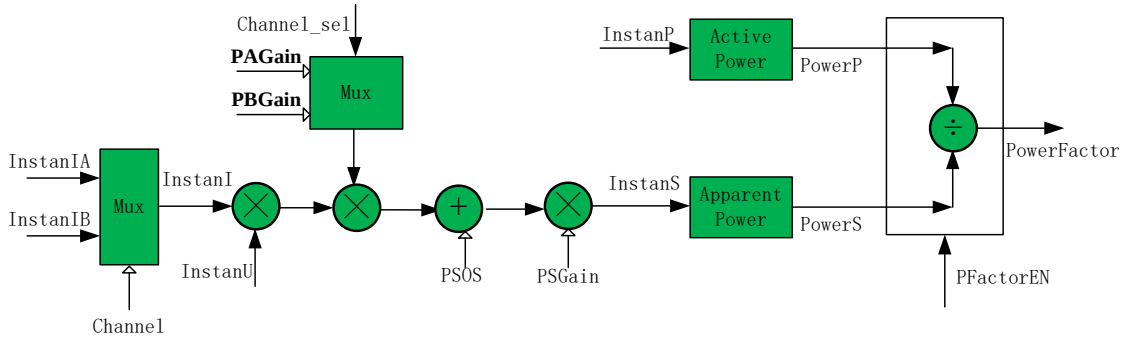


Figure 11 Apparement Power and Factor block diagram

8.8 ACTIVE ENERGY ACCUMULATION

PFCntPA/ PFCntPB, HFConst, Pulse Output, Energy Register Relations:

When | PFCntPA|(or| PFCntPB|)= the register value of HFConst, PFx outputs a pulse. Simultaneous Energy Register Energy_PA or Energy_PB plus 1

The relationship between pulse output, energy register and PArun (PBrun) and PstartPA(PstartPB):

Functional registers and PFx output are also controlled by PArun (PBrun) and PstartPA/PstartPB.

When PArun (PBrun) = 0 or | PowerPx | (PowerPA / PowerPB) is less than the set value of PStartPA / PStartPB register, PFx (INT1 / INT2) does not output pulses, PFCntPx (PFCntPA / PFCPB) and functional register do not increase.

Reverse indication:

When the active power is negative, the REVPA/REVPB bit of EMUStatus register will be changed to 1, and the REVPA/REVPB bit will be updated synchronously with PFx

(INT1/INT2) pulse.

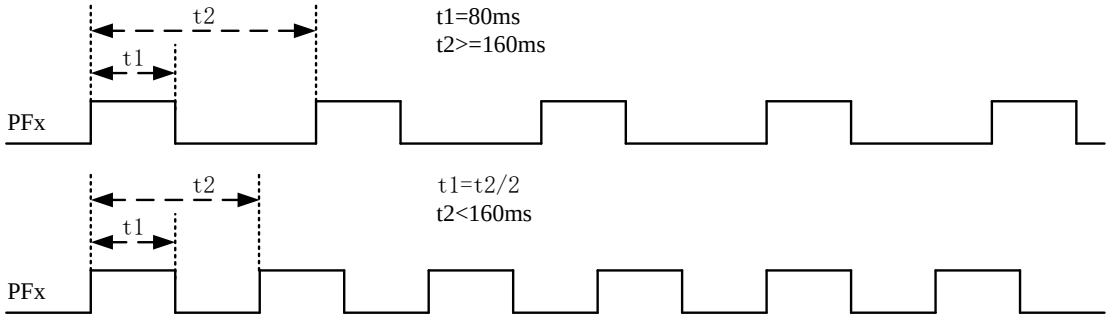


Figure 12 PFx(INT1/INT2) Output Sequence Diagram

NOTE：When the pulse output period is less than 160ms, the pulse is output in the form of 50% duty cycle.

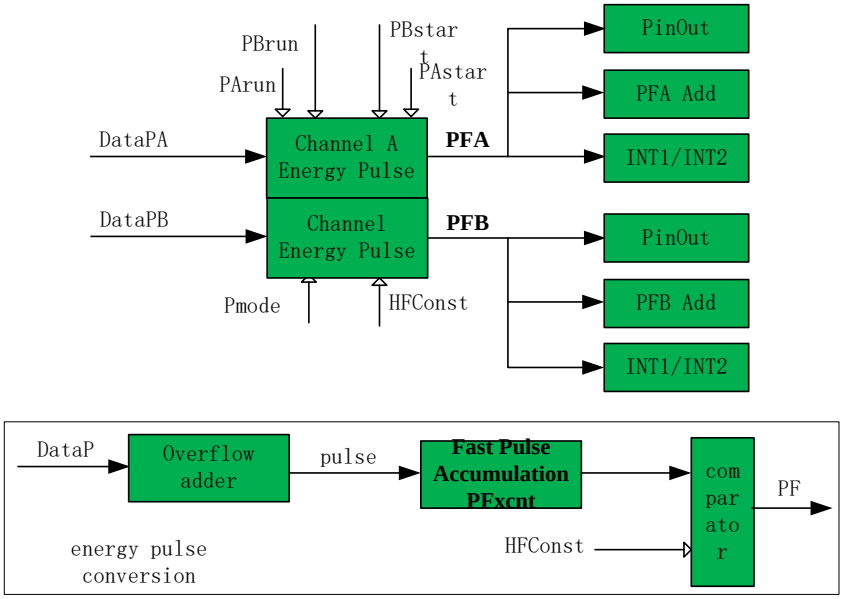


Figure 13 Energy calculation block diagram

8.9 Zero Crossing Detection, Phase Angle and Voltage Frequency Measurement

HLW8110/HLW8112 has zero-crossing detection in voltage channel, current channel A and current channel B. WaveEn = 1 of EMUCON2 register needs to be configured first. Zero-crossing detection can be turned on by configuring ZXEN register of EMUCON2. Four zero-crossing output modes can be selected by configuring ZXD1 and ZXD0 register bits: see Table 8.

Zero-crossing status can be read through IE or IF registers, or INT1/INT2 output

status can be set.

HLW8110/HLW8112 can measure the phase angle between voltage channel and current channel A or B (ZXEN=1 and WaveEn=1 must be configured to measure the phase angle). Register Angle represents the angle between voltage channel and current channel A or current channel B, and the resolution is 0.0805 degrees when the line frequency is 50 Hz; when the line frequency is 60 Hz, the line frequency is 0.0805 degrees. The time resolution is 0.0965 degree.

Formula for calculating phase angle:

Formula 1: Phase angle (50HZ) = Angle*0.0805, unit:degree

Formula 2: Phase angle (60Hz) = Angle*0.0965, unit:degree

The angular register value between current and voltage, the register address is: 0x22H;

When the linear frequency is 50HZ, the phase angle is calculated by formula 1, and when the linear frequency is 60HZ, the phase angle is calculated by formula 2.

If the calculated phase angle data = 25.12, the phase angle = 25.12 degrees.

HLW8110/HLW8112 realizes the measurement of voltage channel frequency (ZXEN=1 and WaveEn=1 must be configured);The fundamental frequency is measured and the bandwidth is 250 Hz. The voltage frequency is determined by reading the value of Ufreq. Ufreq is a 16-bit unsigned number.

The parameter formatting formula is f=clk_sys/8/Ufreq. For example, if the system clock is clk_sys=3.579545MHz and Ufreq=8948, the measured actual frequency is f=3579545/8/8948=49.9908Hz.

The period of updating the measured value of voltage frequency is 0.64 s (voltage frequency is 50 Hz)/0.533 s (voltage frequency is 60 Hz).

$$\text{Line Frequency} = \frac{3579000}{8 * |\text{Ufreq}|}$$

Ufreq: Voltage Line frequency (L line), register address: 0x23H;

If the calculated frequency is 49.99, the linear frequency is 49.99HZ.

Table 8 Zero-crossing Selection Output Table

ZXD1	ZXD0	description
0	0	Select forward zero-crossing point as zero-crossing detection signal and zero-crossing output signal as signal frequency/2
0	1	Negative zero-crossing point is selected as zero-crossing detection signal and zero-crossing output signal is signal frequency/2.
1	0	The positive and negative zero-crossing points are selected as zero-crossing detection signals, and the zero-crossing output signal is signal frequency.
1	1	

Note：The zero-crossing detection of HLW8110/HLW8112 has a certain delay compared with the zero-crossing point of the actual signal: 2.23ms.

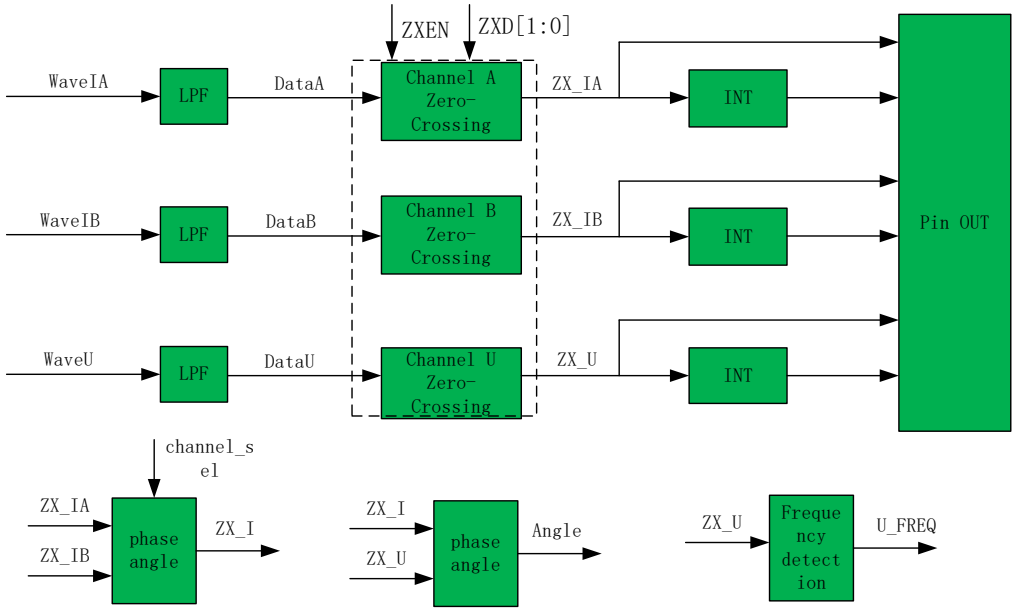


Figure 14 Zero-crossing detection block diagram

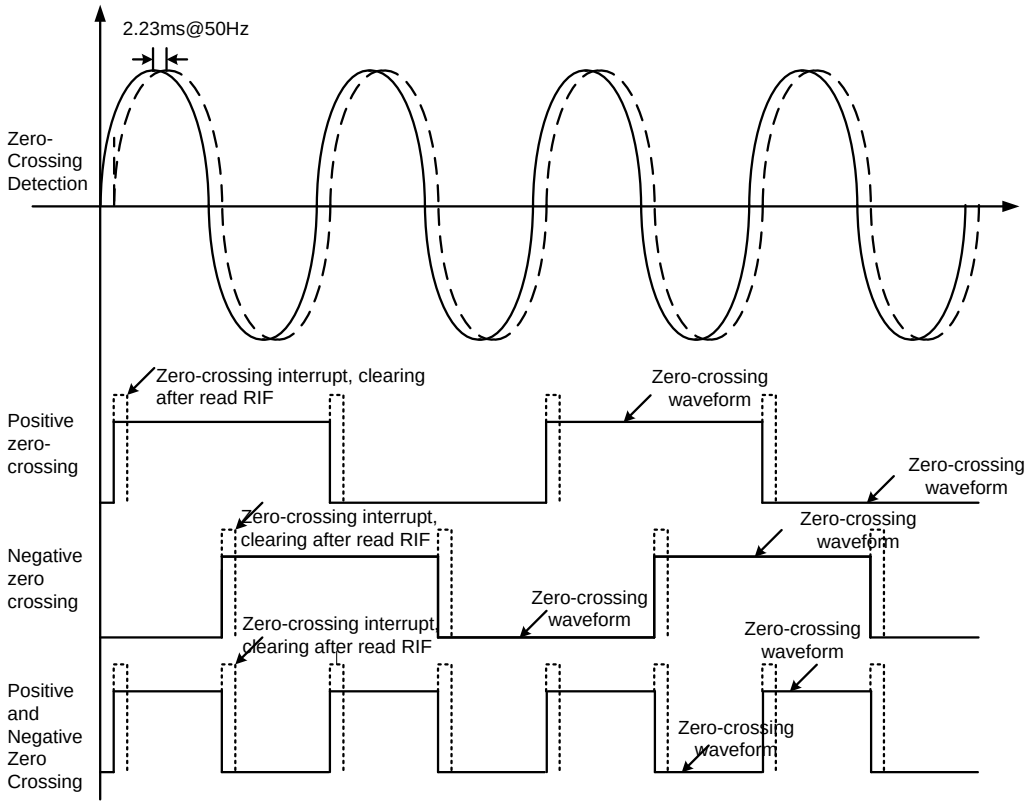


Figure 15 Zero-crossing waveform and interrupt schematic diagram

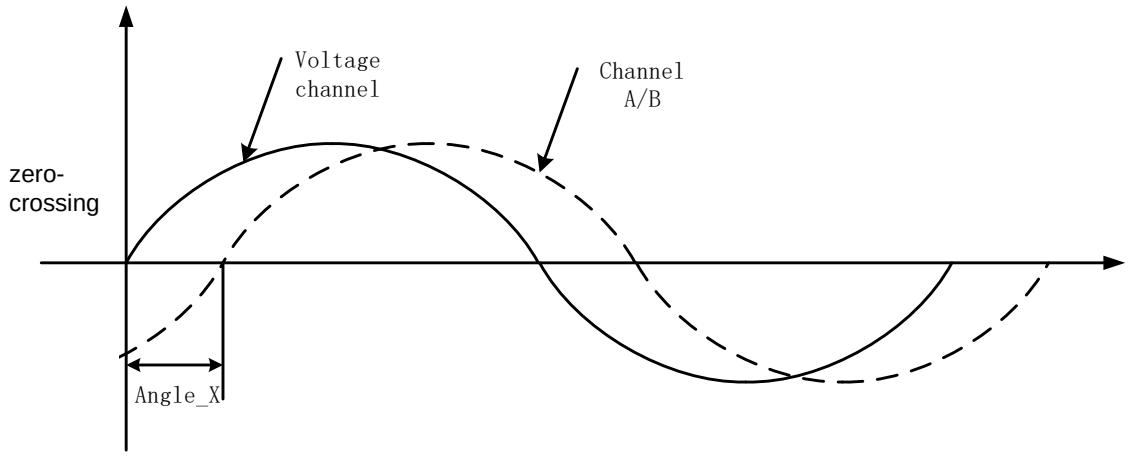


Figure 16 Diagram of phase angle

8.10 Peak detection

Current channel A, current channel B and voltage channel of HLW8110/HLW8112 have peak detection characteristics. It is necessary to turn on instantaneous data function (WaveEn=1 must be configured first) and PeakEN can turn on peak detection function. This feature continuously records the maximum voltage and current waveforms.

Peak detection can be used in conjunction with over-voltage and over-current detection, providing a complete surge detection function (see the current and over-voltage detection section).

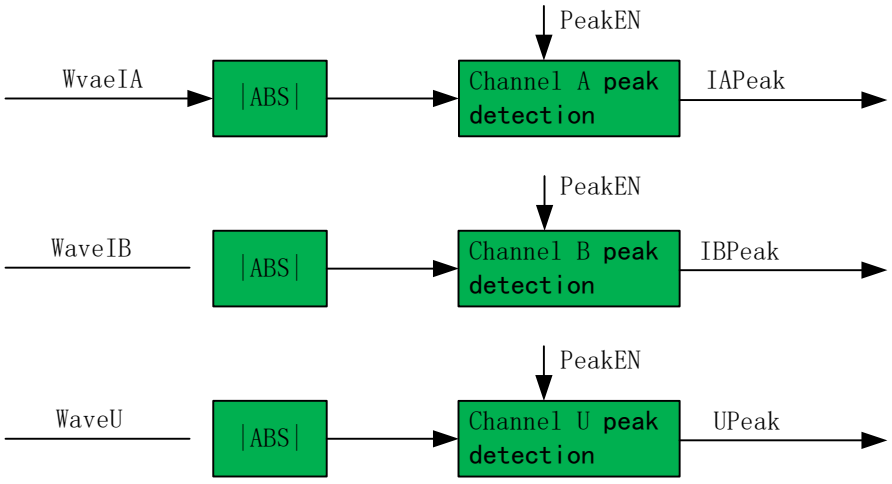


Figure 17 Peak detection block diagram

Peak detection is to obtain instantaneous measurements from the absolute values of current and voltage output waveforms and store them in three 24-bit registers. PeakIA, PeakIB and PekU are the three registers that record the peak values of current channel A, current channel B and voltage channel respectively.

Whenever the absolute values of waveforms exceed the currently stored values in PeakIA, PeakIB and PekU registers, these registers are updated, and reading these registers clears the contents of the corresponding xPEAK registers and restarts peak measurements. The measurement has no relevant time period.

Note: After reading the peak register, we need to wait 10 ms to read the value of the peak register. Otherwise, the peak value read is not necessarily the largest value in half-wave cycle.

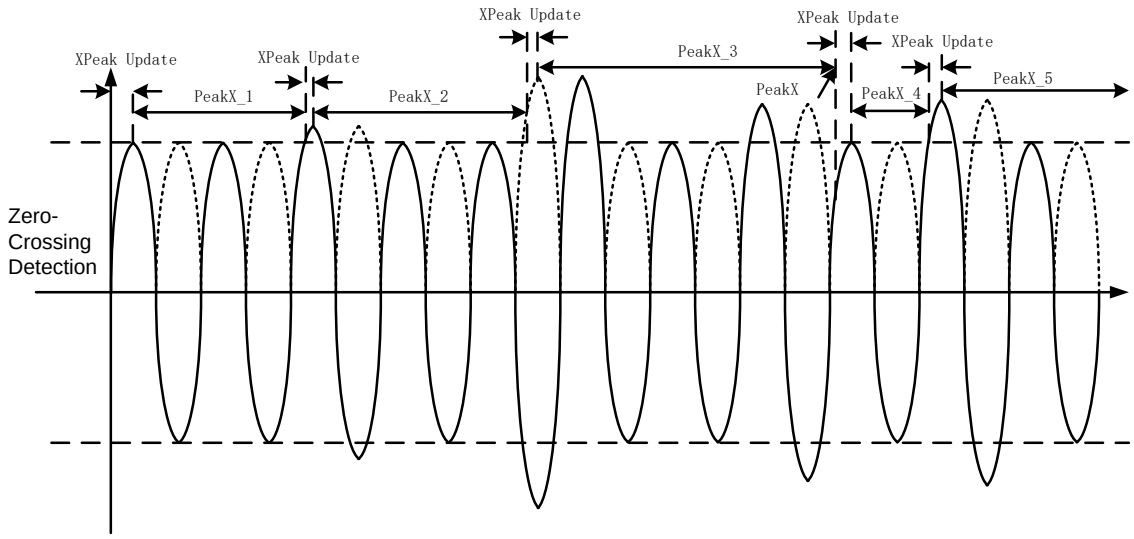


Figure 18 Peak Detection Diagram

8.11 Overcurrent, Overvoltage and Active Power Overload Detection

HLW8110/HLW8112 has the characteristics of over-current, over-voltage and active power overload detection. It can detect whether the absolute values of current waveform, voltage waveform and active power exceed the programmable threshold. OverEn [EMUCON2.bit3] can turn on the functions of over-current, over-voltage and active power overload detection (WaveEN [EMUCON2.5] = 1 needs to be configured first).This feature uses instantaneous current, voltage signals and active power values.

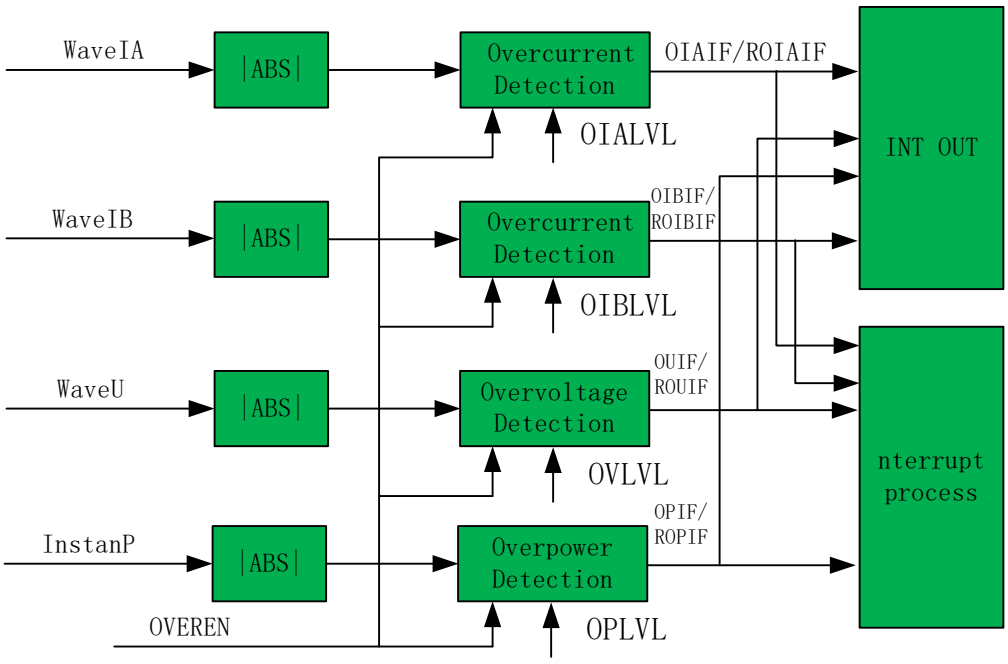


Figure 19 Overload detection block diagram

There are four registers related to this feature: OVLVL, OIALVL, OIBLVL and OPLVL. They are used to set voltage, current channel A, current channel B and active power threshold respectively. They are unsigned registers. The default value of the registers is 0xFFFF, which is aligned with the high 17 bits of WaveIA, WaveIB, WaveU and InstanP. Sexual prohibition. If HLW8110/HLW8112 detects the conditions of over-current, over-voltage and over-power, the relevant bits of IF/RIF registers will output corresponding levels. After reading RIF registers, the bits of corresponding IF registers and RIF registers will be cleared 0. If the corresponding interrupt enable signal is opened, the interrupt signal will be output through IRQ.

There are two ways to calculate the overcurrent threshold of current channel A: applying actual current to calculate the overcurrent threshold or calculating the overcurrent threshold through theoretical formula. Examples are given for calculating the overcurrent threshold of current channel A:

1. If the RmsIA register is RmsIA=0C49BAH (mean value of continuous reading multiple times) when 5A current is applied to current channel A, the overcurrent current of current channel A is set to 10.2A; OIALVL calculation formula is as follows:

OIALVL = RmsIA / 5 * 10.2 * sqrt (2) / 2 ^ 7 = 46E4H.

RmsIA/5*10.2: Register value of RmsIA at 10.2A;

RmsIA/5*10.2*sqrt(2): the corresponding peak at 10.2A;

2 ^ 7: Move the calculated result 7 bits to the right.

2. The overcurrent threshold of current channel A can also be calculated by theoretical method directly.

OIALVL = IA * sqrt (2) * R * 1.5 * PGAIA / Vref * 2 ^ 16.

IA: The RMS of overcurrent needed to be set in A.

R: Sampling resistance of current channel A, in units of_;;;

PGAIA: The PGA amplification factor of current channel A is 16 by default.

Vref: Chip reference voltage output, unit V, typical value of 1.25V;

* 2 ^ 16: The register bit width of OIALVL is 16 bits.

From the above formulas, it can be seen that the influence of sampling resistance R, PGA amplification factor and chip reference Vref error can be eliminated by applying actual current to calculate overcurrent threshold. Current channel B overcurrent threshold and voltage channel overvoltage threshold are similar to current channel A.

There are also two ways to calculate the active power overload threshold: applying actual current and voltage to calculate the overload threshold or calculating the active power overload threshold through theoretical formula. Examples are given for calculating the active power overload threshold.

1. When the current and voltage are applied in current channel A, the power factor is 1 and the active power is 1000W, the value of PowerPA register is PowerPA=2F23872H (average value of continuous reading multiple times), and the active power overload is set to 10500W. The OPLVL formula is as follows:

OPLVL = PowerA / 1000 * 10500 / 2 ^ 15 = 3DDEH.

PowerA/1000*10500: Register value of PowerPA at 10500W;

/ 2 ^ 15: Move the calculated result 15 bits to the right.

2. Active power overload threshold can also be calculated by theoretical method directly.

OPLVL = IA * Ria * U * Ru * 2.25 * PGAIA * PGAU / Vref ^ 2 * 2 ^ 16.

IA: The current RMS corresponding to active over-current and overload should be set in A.

IA: The effective value of the voltage corresponding to the active over-current overload, in V, should be set.

Ria: Sampling resistance of current channel A, in units ofΩ;

Ru: The sample resistance ratio of the voltage channel is 1 k/(1M+1k).

PGAIA: The PGA amplification factor of current channel A is 16 by default.

PGAU: PGA amplification factor of voltage channel, default 1;

Vref: Chip reference voltage output, unit V, typical value of 1.25V;

* 2 ^ 16: The register bit width of OPLVL is 16 bits.

From the above formulas, it can be seen that applying actual current and voltage to calculate active power overload threshold can eliminate the influence of sampling resistance Ria/Ru, PGAIA and PGAU amplification factor, chip reference Vref error.

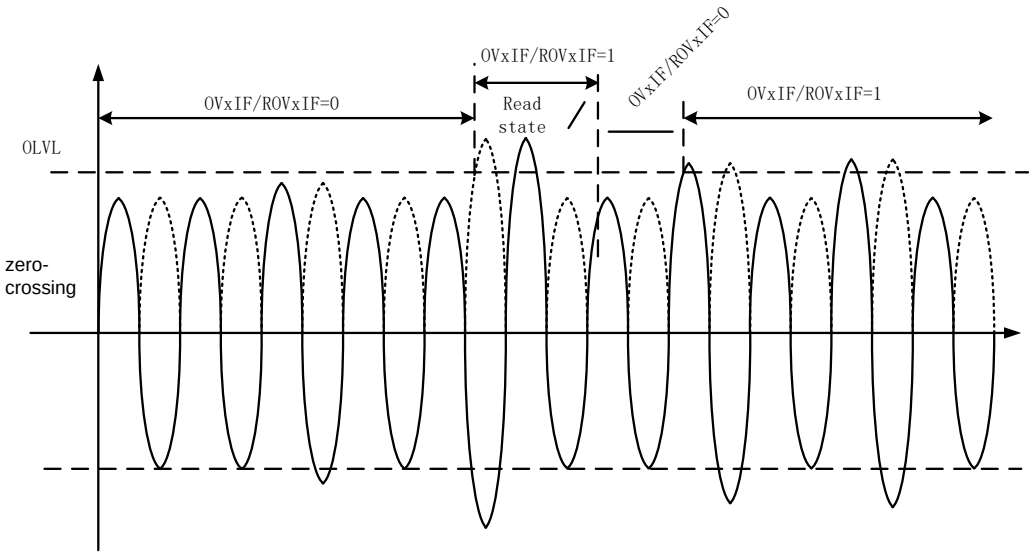


Figure 20 Overvoltage Overcurrent Overload and Power Detection Diagram

8.12 Voltage drop detection

HLW8110/HLW8112 has the characteristics of voltage sag detection. By configuring SAGEN, the function of voltage sag detection can be turned on (WaveEN=1 must be configured first). When the absolute value of line voltage falls below the programmable threshold and continues the programmable number of line cycles, the user will be reminded. This feature can provide early warning signal of line voltage loss. Voltage sag characteristics are controlled by two registers: SAGCYC (unsigned number) and SAGLVL (unsigned number). These registers control the sag period and the sag voltage threshold respectively. If a voltage sag occurs, the sag position is set to 1, and the SAG will be cleared after reading.

Set up the SAGCYC register:

16-bit unsigned SAGCYC registers contain programmable plunge cycles, only 8-bit lower valid. The period of sag refers to the number of half-wave cycles. When the number is less than that, the voltage channel must remain unchanged. Only when the number exceeds or equals to that number, can a sag occur. The 1 LSB of SAGCYC register corresponds to 1 half-wave period. The maximum value of SAGCYC register is 255.

At 50 Hz, the longest period of sag is 2.55 seconds.

At 60 Hz, the longest period of sag is 2.125 seconds.

When this feature is enabled, the new SAGCYC cycle takes effect immediately if the SAGCYC value is changed. Therefore, a sudden drop event can be triggered by a combination of multiple periods. Before writing new periodic values to SAGCYC registers, in order to prevent overlap, SAGLVL registers should be reset to 0 to effectively disable this feature.

Set up the SAGLVL register:

The 16-bit SAGLVL register contains the voltage amplitude, and the voltage channel must be reduced below that amplitude before a sudden drop can occur. Each LSB of the register is mapped to the peak value register of the voltage channel accurately, so the magnitude can be set according to the peak reading of the voltage channel. To set up SAGLVL registers, nominal voltage should be applied. After waiting for several line cycles, the PeakU register is read to determine the voltage input, and then the reading is scaled to the magnitude required for sag detection. For example, if the threshold drop is required to be 80% of the nominal voltage, the peak reading should be obtained and the value equal to 80% of the reading should be written into the SAGLVL register. This method ensures that precise SAGLVL values are obtained for specific designs.

Voltage sag interruption:

The voltage sag detection characteristics of HLW8110/HLW8112 have a related interrupt SAGIF. If this interruption is enabled, the voltage sag event will turn the external IRQ pin into a low level. This interrupt is disabled by default. There are two ways to calculate the undervoltage threshold of the voltage channel: applying actual voltage to calculate the undervoltage threshold or calculating the undervoltage threshold through theoretical formula, and calculating the voltage undervoltage threshold with examples:

1. When 220 V voltage is applied to the voltage channel, the RmsU register value is RmsU=21C21CH (the average value of continuous reading multiple times), and the voltage undervoltage is set to 220 V*60%=132V. The SAGLVL formula is as follows:

SAGLVL=RmsU/220*132*sqrt(2)/2^7=3947H。

RmsU/220*132： Register value of RmsU at 132V；

RmsU/220*132*sqrt(2)： Peak value corresponding to 132V；

2^7：Move the calculated result to the right by 7 bits.。

2、The undervoltage threshold of voltage channel can also be calculated directly by theoretical method.：

SAGLVL=U* sqrt(2)*Ru*1.5*PGAU/Vref*2^16。

U： The effective value of voltage undervoltage to be set in V；

Ru：Sampling resistance ratio of voltage channel, typical value 1kΩ/（1MΩ+1kΩ）；

PGAU： PGA Amplification Factor of Current Channel A, default 1；

Vref： Chip reference voltage output, unit V, typical value 1.25V；

2^16： The register bit width of SAGLVL is 16 bits；

From the above formulas, it can be seen that the influence of sampling resistance Ru, PGAU amplification factor and chip reference Vref error can be eliminated by applying actual current to calculate overcurrent threshold.

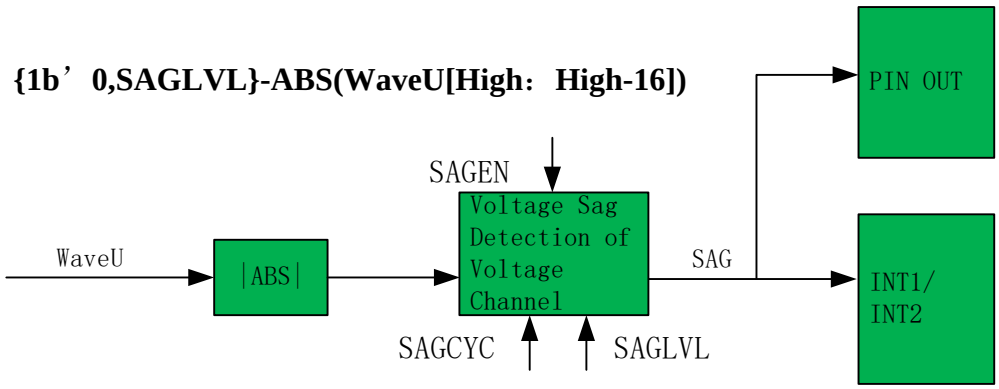


Figure 21 Voltage drop detection block diagram

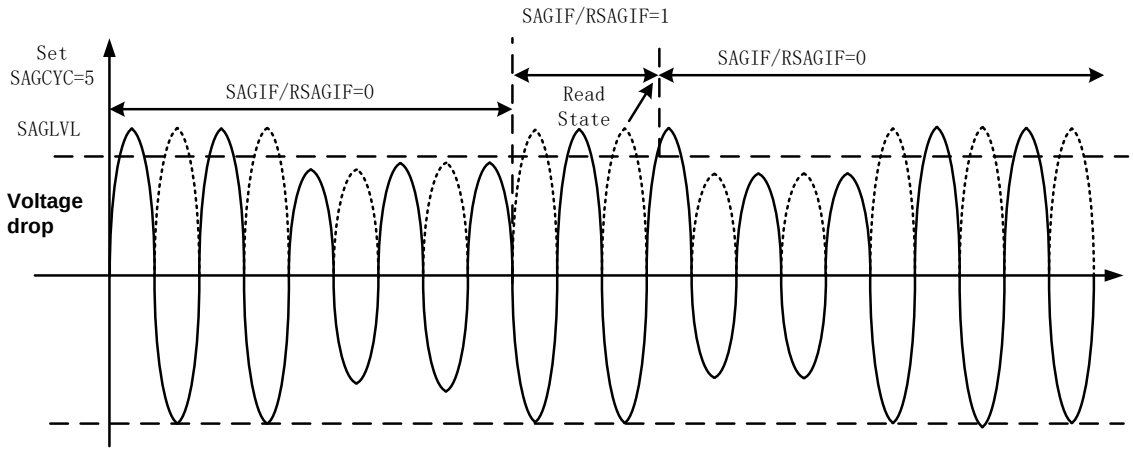


Figure 22 Voltage drop detection chart

8.13 Mean signal

HLW8110/HLW8112 provides mean signals, which include current channel A RMS, current channel A RMS, voltage RMS, active power of channel A, active power of channel B, apparent power and power factor. All mean registers except 32-bit signed registers are 24-bit bands. Symbol register. All measurements are updated at a rate of 3.4 Hz, 6.8 Hz, 13.6 Hz and 27.2 Hz.

HLW8110/HLW8112 provides a mean interrupt status bit, which enables the measurement to synchronize with the mean signal update rate, and the status bit will be cleared after reading.

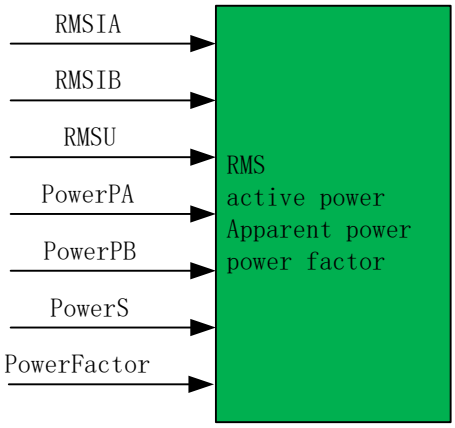


Figure 23 Avarge data block diagram

8.14 Instantaneous signal and sampling waveform

HLW8110/HLW8112 not only provides instantaneous voltage RMS, current RMS, active power and apparent power (instantaneous data output function can be turned on by using WaveEN), but also provides waveform data of voltage and current channels (instantaneous data output function can be turned on by configuring WaveEN). Using this information, instantaneous data can be analyzed in more detail, including reconstructing current and voltage inputs for harmonic analysis.

The measurement results of instantaneous voltage RMS, current RMS and instantaneous waveform data are provided by a set of 24-bit signed registers, and instantaneous active power and apparent power are provided by a set of 32-bit signed registers. All measurements were updated at a rate of 6.99 kHz (CLKIN/512).

HLW8110/HLW8112 provides an instantaneous interrupt status bit, which triggers at a rate of 6.99 kHz, enabling the measurement to synchronize with the instantaneous signal update rate, which will be cleared after reading.

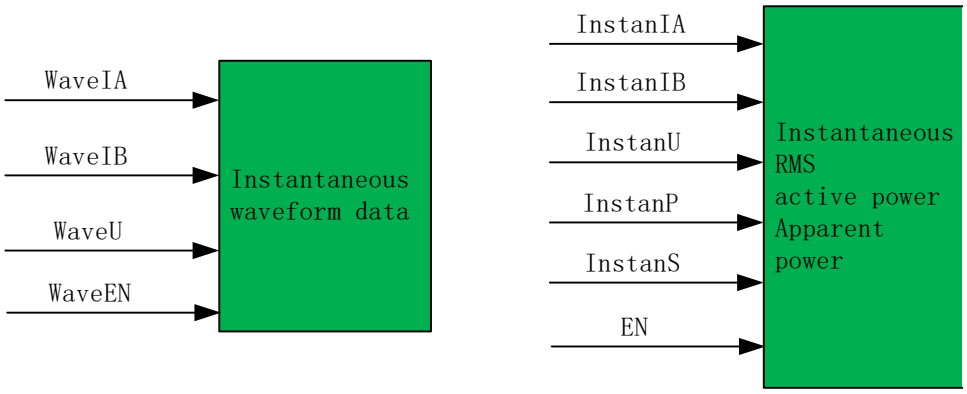


Figure 24 Instantaneous signal and waveform data block diagram

8.15 Temperature sensor

HLW8110/HLW8112 Current Channel B also provides internal temperature detection, which can convert the output voltage of temperature sensor into 24-bit AD value through ADC and digital filtering and store it in RmsIB register.

The calibration steps of HLW8110/HLW8112 temperature sensor are as follows:

1、Configure ADC2ON = 1 (Open channel B ADC)、PGAIB[2:0]=000B；

2、Configure Tensor_en=1 (turn on temperature module), HPFIBOFF=1 (turn off B-channel high-pass filter)；

3、Configure Tsensor_Step [1:0]= 00B to read RmsIB register values (recommended four consecutive reads for averaging) and record register values as D1；

4、Configure Tsensor_Step [1:0]= 01B to read RmsIB register values (recommending four consecutive reads for averaging), and register values are recorded as D2；

5、Configure Tsensor_Step [1:0]= 10B to read RmsIB register values (recommending four consecutive reads for averaging). Register values are recorded as D3；

6、Configure Tsensor_Step [1:0]= 11B to read RmsIB register values (recommended four consecutive reads for averaging) and record register values as D4；

7、Add D1, D2, D3 and D4 to get D0 on average.：D0=(D1+D2+D3+D4)/4；

Because of the change of process parameters, temperature sensors need to be calibrated. The calibration method is as follows:：

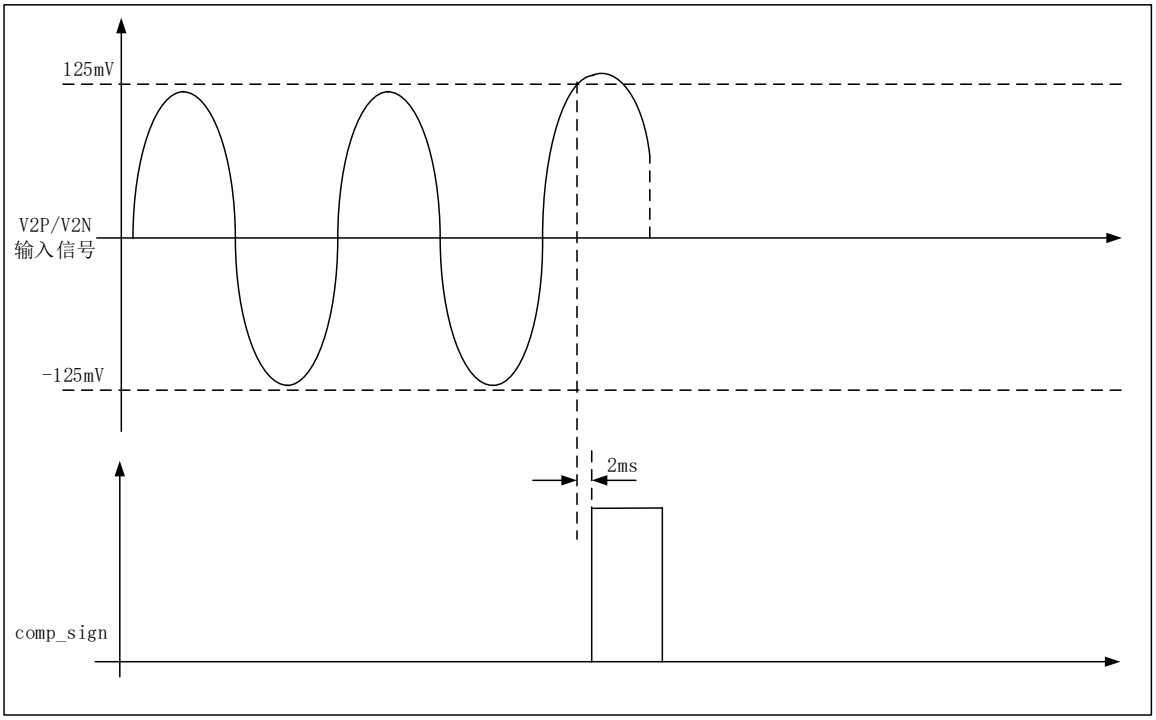
Set the calibration temperature to Tc (unit temperature, such as 25 C). According to step 3-7, the average value is Dc. Store the Dc value in the storage unit. Then the temperature coefficient Tr = Dc/(273.15+Tc).

In practical use, the average D at the current temperature is obtained by step 3-7 test, and the current temperature (unit temperature) is calculated according to the following formula.

$$T = \frac{D(Tc + 273.15)}{D_c} - 273.15$$

8.16 Comparator

HLW8112 current channel B can also be used as the signal input of the comparator. When the peak value of the input signal exceeds the threshold set by the internal comparator 125 mV, the comparator will output a high level. The output signal of the comparator can be output directly through INT1/INT2 or through interruption.



The steps of using HLW8112 comparator are as follows:

1、Configure INT1 or INT2 = 010B and output comparative signals through INT1 or INT2.

2、Configure comp_off=1 (the comparator is working)；

When the comp_sign signal is detected to be high, the external power supply needs to be disconnected, and HLW8112 can be re-energized to work properly.

9 Register description

The list of registers for HLW8110/HLW8112 is shown in Table 9.

Table 9 Register List

Addr	Name	Bytes	Reset Value	Description	Write Protection	R/W
Calibration parameters and metering control registers						
00H	SYSCON	2	0A04h	System Control Register	Yes	R/W
01H	EMUCON	2	0000h	Energy Measure Control Register	Yes	R/W
02H	HFConst	2	1000h	Pulse Frequency Register	Yes	R/W
03H	Pastart	2	0060h	Active Start Power Setting of Channel A	Yes	R/W
04H	Pbstart	2	0060h	Active Start Power Setting of Channel B	Yes	R/W
05H	PAGain	2	0000h	Channel A Power Gain Calibration Register	Yes	R/W
06H	PBGain	2	0000h	Channel B Power Gain Calibration Register	Yes	R/W
07H	PhaseA	1	00h	Channel A Phase Calibration Register	Yes	R/W
08H	PhaseB	1	00h	Channel B Phase Calibration Register	Yes	R/W
0AH	PAOS	2	0000h	Channel A Active Power Offset Calibration	Yes	R/W
0BH	PBOS	2	0000h	Channel B Active Power Offset Calibration	Yes	R/W
0EH	RmsIAOS	2	0000h	Current Channel A RMS Offset Compensation	Yes	R/W
0FH	RmsIBOS	2	0000h	Current Channel B RMS Offset Compensation	Yes	R/W
10H	IBGain	2	0000h	Current Channel B Gain Settings	Yes	R/W
11H	PSGain	2	0000h	Apparent power gain calibration	Yes	R/W
12H	PSOS	2	0000h	Visual Power Offset Compensation	Yes	R/W
13H	EMUCON2	2	0001h	Meter Control Register 2	Yes	R/W

14H	DCIA	2	0000h	IA Channel DC offset Correction Register	Yes	R/W
15H	DCIB	2	0000h	IB Channel DC offset Correction Register	Yes	R/W
16H	DCIC	2	0000h	U Channel DC offset Correction Register	Yes	R/W
17H	SAGCYC	2	0000h	Voltage sag period setting	Yes	R/W
18H	SAGLVL	2	0000h	Voltage sag threshold setting	Yes	R/W
19H	OVLVL	2	FFFFh	Voltage Overvoltage Threshold Setting	Yes	R/W
1AH	OIALVL	2	FFFFh	Current Channel A Overcurrent Threshold Setting	Yes	R/W
1BH	OIBLVL	2	FFFFh	Current Channel B Overcurrent Threshold Setting	Yes	R/W
1CH	OPLVL	2	FFFFh	Threshold setting of active power overload	Yes	R/W
1DH	INT	2	3210h	INT1/INT2 interrupt set defaults to output PFA defaults to output PFB	Yes	R/W
Metrer parameter and status register						
20H	PFCntPA	2	0000h	Fast Combination Active Pulse Counting of Channel A	Yes	R/W
21H	PFCntPB	2	0000h	Fast Combination Active Pulse Counting of Channel B	Yes	R/W
22H	Angle	2	0000h	The angle between current and voltage is selected by command: Current Channel A Phase Angle with Voltage Channel or Phase Angle with Current Channel B and Voltage Channel	-	R
23H	Ufreq	2	0000h	Voltage Frequency (L Line)	-	R
24H	RmsIA	3	000000h	IARms	-	R

25H	RmsIB	3	000000h	IBRms	-	R
26H	RmsU	3	000000h	URms	-	R
27H	Power Factor	3	7FFFFFh	Power Factor Register, Selected by Command: Channel A Power Factor or Power Factor of Channel B		
28H	Energy_PA	3	000000h	Channel A active power, default to zero after reading, can be configured to zero after reading.	-	R
29H	Energy_PB	3	000000h	Channel B active power, default to zero after reading, can be configured to zero after reading.	-	R
2CH	Power PA	4	00000000h	Active power of channel A, update rate 3.4 Hz, 6.8 Hz, 13.6 Hz, 27.2 Hz	-	R
2DH	Power PB	4	00000000h	Active power of channel B, update rate 3.4 Hz, 6.8 Hz, 13.6 Hz, 27.2 Hz	-	R
2EH	Power S	4	00000000h	The apparent power of channel A or B is selected by command. Updating rates of 3.4 Hz, 6.8 Hz, 13.6 Hz and 27.2 Hz	-	R
2FH	EMU Status	3	00B32Fh	Measurement Status and Check and Register	-	R
30H	PeakIA	3	000000h	Peak of Current Channel A	-	R
31H	PeakIB	3	000000h	Peak of Current Channel B	-	R
32H	Peak U	3	000000h	Peak Value of Voltage Channel U	-	R
33H	InstanIA	3	000000h	Current Channel A Instantaneous Value	-	R

34H	InstanIB	3	000000h	Current Channel B Instantaneous Value	-	R
35H	InstanU	3	000000h	Instantaneous Value of Voltage Channel	-	R
36H	WaveIA	3	000000h	Current Channel A Waveform		R
37H	WaveIB	3	000000h	Current Channel B Waveform		R
38H	WaveU	3	000000h	Voltage Channel Waveform		R
3CH	InstanP	4	00000000h	Active power instantaneous value, select channel A by Command Or the instantaneous value of active power in channel B,	-	R
3DH	InstanS	4	00000000h	Depending on the instantaneous power value, channel A is selected by command. Or the instantaneous real power of channel B,	-	R
Interrupt register						
40H	IE	2	0000h	Interrupt admission register	Yes	R/W
41H	IF	2	0000h	Interrupt flag register (not writable)	-	R
42H	RIF	2	0000h	Reset the interrupt status register and clear it after reading	-	R
System Status Register						
43H	SysStatus	1	--	System Status Register	-	R
44H	Rdata	4	--	Data read by SPI last time	-	R
45H	Wdata	2	--	Data written by the last SPI	-	R
6FH	Coeff_chksum	2	FFFFh	Coefficient checksum		

70H	RmsIAC	2	FFFFh	Current Channel A RMS Conversion Coefficient	-	R
71H	RmsIBC	2	FFFFh	Current Channel B RMS Conversion Coefficient	-	R
72H	RmsUC	2	FFFFh	U-RMS Conversion Coefficient of Voltage Channel	-	R
73H	PowerPAC	2	FFFFh	Active Power Conversion Coefficient of Current Channel A	-	R
74H	PowerPBC	2	FFFFh	Active Power Conversion Coefficient of Current Channel B	-	R
75H	PowerSC	2	FFFFh	Apparent power conversion coefficient	-	R
76H	EnergyAC	2	FFFFh	Energy Conversion Coefficient of A Channel	-	R
77H	EnergyBC	2	FFFFh	Energy Conversion Coefficient of B Channel	-	R

Note: For a write-protected register, when writing input data to the register, write enable command first.
The addresses not listed in the list are all 16Bit, not writable, read out to 0;

9.1 Calibration parameter register

9.1.1 System Control Register

Table 10 System Control Register

SYSTEM Control Register（SYSCON） Addr:0x00H default：0A04H		
Bit	Name	Description
15-12	NC	NC
11	ADC3ON	=1， Open voltage channel U =0， Close voltage channel U
10	ADC2ON	=1，Open current channel B =0，Close current channel B
9	ADC1ON	=1，Open current channel A =0，Close current channel A
8-6	PGAIB[2:0]	Setting Current Channel B Gain： PGAIB[2:0]=1XX， PGA=16 PGAIB[2:0]=011， PGA=8 PGAIB[2:0]=010， PGA=4 PGAIB[2:0]=001， PGA=2

		PGAIB[2:0]=000， PGA=1
5-3	PGAU[2:0]	Setting Voltage Channel U Gain: PGAU[2:0]=1XX， PGA=16 PGAU[2:0]=011， PGA=8 PGAU[2:0]=010， PGA=4 PGAU[2:0]=001， PGA=2 PGAU[2:0]=000， PGA=1
2-0	PGAIA[2:0]	Setting Current Channel A Gain： PGAIA[2:0]=1XX，电流通道 A 的 PGA=16 PGAIA[2:0]=011，电流通道 A 的 PGA=8 PGAIA[2:0]=010，电流通道 A 的 PGA=4 PGAIA[2:0]=001，电流通道 A 的 PGA=2 PGAIA[2:0]=000，电流通道 A 的 PGA=1

9.1.2 Meter Control Register

Table 11 Meter Control Register

Energy Measure Control Register(EMUCON) Addr:0x01H default:0000H		
Bit	Name	Description
15-14	Tsensor_Step[1:0]	Measuring steps of temperature sensor: = 00, the first step of temperature sensor measurement, OP1, OP2 Offset is +/+; = 01, the second step of temperature sensor measurement, OP1, OP2 Offset is +/-. = 10, the third step of temperature sensor measurement, OP1, OP2 Offset is - /+. = 11, the fourth step of temperature sensor measurement, OP1, OP2 Offset is - /-. The current measured temperature can be obtained by averaging the four results.
13	tensor_en	Temperature measurement module = 0, Close the temperature measurement module = 1,Open the temperature measurement module
12	comp_off	The comparator module opens or closes: = 0, the comparator module is in working state = 1,The comparator module is closed Comparator function and B-channel current measurement can only be one of two choices

11-10	Pmode[1:0]	Active power calculation method: Pmode = 00, both positive and negative active power are involved in the accumulation. The accumulation mode is algebraic and mode, and the reverse active power is indicated by REVQ symbols. Pmode = 01, only positive active power is accumulated. Pmode = 10, both positive and negative active power are involved in the accumulation. The accumulation mode is absolute value mode, and there is no reverse active power indication. Pmode = 11, reserved, the same as Pmode = 00
9	DC_MODE	RMS Calculate Mode: = 0, working in normal working mode, for AC measurement; = 1, Work in through mode: turn off self-multiplication, LPF and open-side operation; In through mode, WaveEn = 1 needs to be turned on
8	ZXD1	Different waveforms are output according to the configuration of ZXD1 and ZXD0: = 0，The ZX output changes only at the selected zero crossing point, refer to ZXD0 = 1，ZX output changes at both positive and negative zero-crossing points
7	ZXD0	= 0, Select forward zero-crossing point as zero-crossing detection signal = 1, Select the negative zero-crossing point as the zero-crossing detection signal
6	HPFIBOFF	= 0, Open current channel B digital high-pass filter for AC measure = 1, Close current channel B digital high-pass filter for DC measure
5	HPFIAOFF	= 0, Open current channel A digital high-pass filter for AC measure = 1, Close current channel A digital high-pass filter for DC measure
4	HPFUOFF	= 0, Open voltage channel U digital high-pass filter for AC measure = 1, Close voltage channel U digital high-pass filter for DC measure
3-2	NC	-
1	PBRUN	PBRUN = 1, turn on PFB pulse output and Energry_PB register accumulation PBRUN = 0 (default), turn off PFB pulse output and turn off Energry_PB register accumulation
0	PARUN	PARUN = 1, turn on PFA pulse output and Energry_PA register accumulation PARUN = 0 (default), turn off PFA pulse output and turn off Energry_PA register accumulation

9.1.3 Energy Measure Control Register2

Table 12 Energy Measure Control Register2

<table>
<tr><td colspan="3">Energy Measure Control Register2(EMUCON2) Addr:0x13H default：0001H</td></tr>
<tr><td>Bit</td><td>Name</td><td>Description</td></tr>
<tr><td>15</td><td>-</td><td>-</td></tr>
<tr><td>14-13</td><td>-</td><td>-</td></tr>
<tr><td>12</td><td>SDOCmos</td><td>= 1, SDO pin CMOS open-leak output
= 0, SDO pin CMOS output</td></tr>
<tr><td>11</td><td>EPB_CB</td><td>Energy_PB Clearance Signal Control, default 0
= 1, Energy_PB is not clear after reading.
= 0, Energy_PB clears after reading;</td></tr>
<tr><td>10</td><td>EPA_CA</td><td>Energy_PA Clearance Signal Control, default 0
= 1, Energy_PA is not clear after reading.
= 0, Energy_PA clears after reading;</td></tr>
<tr><td>9-8</td><td>DUPSEL[1:0]</td><td>Frequency of data updates
<table>
<tr><td>DUPSEL</td><td>Frequency</td><td>DUPSEL</td><td>Frequency</td></tr>
<tr><td>00</td><td>3.4Hz</td><td>10</td><td>13.65Hz</td></tr>
<tr><td>01</td><td>6.8Hz</td><td>11</td><td>27.3Hz</td></tr>
</table></td></tr>
<tr><td>7</td><td>CHS_IB</td><td>Current Channel B Measurement Selection Signal
=1 ,Measure IB channel current
=0 ,Measure the temperature inside the chip. It can not used to measure IB channel current.</td></tr>
<tr><td>6</td><td>PfactorEN</td><td>= 1, Turn on the power factor output function
= 0, turn off power factor output function</td></tr>
<tr><td>5</td><td>WaveEN</td><td>= 1, Open waveform data and instantaneous data output function
= 0, Close waveform data and instantaneous data output function</td></tr>
<tr><td>4</td><td>SAGEN</td><td>Voltage sag detection enabling signal, need to configure WaveEN = 1
= 1,Turn on voltage sag detection function
= 0, turn off voltage sag detection function</td></tr>
<tr><td>3</td><td>OverEN</td><td>Overvoltage, Overcurrent and Overload Detection, WaveEN = 1 should be configured first
= 1, Turn on the functions of overvoltage, overcurrent and overload detection.
= 0,Turn off the functions of over-voltage, overcurrent and</td></tr>
</table>

		over-load detection
2	ZxEN	Zero-crossing detection, phase angle and voltage frequency measurement enable signal.WaveEN = 1 needs to be configured first = 1, Turn on zero-crossing detection, phase angle, voltage and frequency measurement functions. = 0, turn off zero-crossing detection, phase angle, voltage frequency measurement function
1	PeakEN	Peak detection enabling signal,WaveEN = 1 needs to be configured first = 1, Turn on peak detection = 0, turn off peak detection function
0	VrefSel	Built-in reference voltage selection = 0,Invalid = 1,Select 1.25V built-in reference voltage

9.1.4 **HFConst Register**

Table 13 HFConst Register

HFConst	Addr:0x02H default:1000H		
W/R	Bit15	Bit14……Bit1	Bit0

HFConst is a 16-bit unsigned number.

When comparing it with PFCNT (PFCnt_PA/PFCnt_PB) register, if PFCNT (PFCnt_PA/PFCnt_PB) is greater than or equal to the value of HFConst, then PF (INT1/INT2) pulse output will occur.

Note: The maximum value of HFConst is 0xffff.

9.1.5 PstartPA、PstartPB

Table 14 PstartPA Register

PstartPA	Addr:0x03H default:0060H		
W/R	Bit15	Bit14……Bit1	Bit0

Table 15 PstartPB Register

PstartPB	Addr:0x04H default:0060H		
W/R	Bit15	Bit14……Bit1	Bit0

Active power without load is configured by PstartPA/PstartPB registers. PstartPA/PstartPB is 16-bit unsigned number. When compared, it is compared with the

absolute value of 24 bits high of PowerPA (32 bits signed number) for starting judgment; | PowerPA (PowerPB)|>> 8(Select high 24bits) is considered to be active potential when it is less than PstartPA (PstartPB). In active latent state, PFA and PFB have no output, energy registers do not update (Energy_PA, Energy_PB), power factor changes to 7FFFFF (PF=1.0), but the values of two active power registers, two current registers, voltage registers and apparent power registers maintain normal output.

In order to improve sensitivity, this value can also be set to 50% of the starting power required by industry standards.

9.1.6 Active Power and Apparent Power Gain Correction Register

Table 16 PAGain/PBGain/PSGain

PAGain	Addr:0x05H default:0000H		
W/R	Bit15	14……1	Bit0

PBGain	Addr:0x06H default:0000H		
W/R	Bit15	14……1	Bit0

PSGain	Addr:0x11H default:0000H		
W/R	Bit15	14……1	Bit0

It consists of three registers: PAGain, PBGain and PSGain, which are in binary complement format with the highest bit being the symbol bit. PAGain is used for the gain calibration of active power in current channel A and voltage channel; PBGain is used for the gain calibration of active power in current channel B and voltage channel; PSGain is used for the gain calibration of apparent power in choosing the energy measurement path;

The calibration range of PAGain and PAGain is (+100%). The calibration range of PSGain is limited by PAGain or PBGain:

- 100%<= PSGain+PAGain (when channel selection is current channel A) or PSGain+PBGain (when channel selection is current channel B)<=+100%. For example, when PAGain = 16'hFAFB, PSGain can gain to 16'h7FFF maximum and negative gain to 16'h8505 minimum. When 16'h8504 will cause spillover.

Before calibration, the power value is P 0, and after calibration, P 1 = P 0* (1 + Gain / 2 ^ 15).

For current channel A, Gain = PAGain;

For current channel B, Gain = PBGain;

For apparent power, Gain = PSGain + PAGain or PSGain + PBGain.

9.1.7 Phase calibration Register

Table 17 Phase calibration Register

PhaseA	Addr:0x07H default:00H	
W/R	Bit7	Bit6…Bit0
	symbol	data

PhaseB	Addr:0x08H default:00H	
W/R	Bit7	Bit6…Bit0
	symbol	data

PhaseA is the phase calibration register of current channel A and voltage channel U, and PhaseB is the phase calibration register of current channel B and voltage channel U. The two registers are symbolic binary complements. Bit7 is the symbol bit, and the phase calibration range is -2.575 +2.575 at 50Hz and -3.09 +3.09 at 60Hz.

1 LSB stands for delay of 1/895KHz = 1.12us/LSB. At 50Hz, 1 LSB stands for 1.12 us*360 degree*50/10^6=0.0201 degree/LSB. At 60Hz, 1 LSB stands for 1.12 us*360 degree*60/10^6=0.0241 degree/LSB.

9.1.8 Active and apparent power Offset calibration registers PA0S and PBOS

Table 18 Active and apparent power Offset calibration registers PA0S and PBOS

PA0S	Addr:0x0AH default:0000H		
W/R	Bit15	14……1	Bit0

PBOS	Addr:0x0BH defult:0000H		
W/R	Bit15	14……1	Bit0

PSOS	Addr:0x12H defult:0000H		
W/R	Bit15	14……1	Bit0

Active Offset calibration is suitable for small signal accuracy calibration. All three registers are in binary complement format, with the highest bit being the symbol bit.

PAOS register is the active power Offset calibration value of current channel A and U channel, and PBOS register is the active power Offset calibration value of current channel B and U channel.

PSOS registers are the Offset calibration values for power.

9.1.9 Current RMS Offset calibration Register

Table 19 IRMS Offset calibration Register

RmsIA0S	Addr:0x0EH default:0000H		
W/R	Bit15	Bit14……Bit1	Bit0

RmsIBOS	Addr:0x0FH default:0000H		
W/R	Bit15	Bit14……Bit1	Bit0

RMS Offset calibration register is used to calibrate the small signal accuracy of RMS. Both registers are in binary complement format, with the highest bit being the symbol bit.

RmsIAOS register is the current A RMS Offset calibration value, and RmsIBOS register is the current B RMS Offset calibration value.

9.1.10 Current Channel B Gain Settings

Table 20 IBGain register

IBGain	Addr:0x10H defult:0000H		
W/R	Bit15	Bit14……Bit1	Bit0

Current channel B gain setting register is used for consistency calibration of two current channels. The consistency calibration is at 100% Ib. The method of use is shown in the method of proofreading.

The current gain register of channel B is in the form of binary complement code, the highest bit is the symbol bit, indicating the range (-1,+1).

If IBGain >= 2 ^ 15, then GainI2= (IBGain-2 ^ 16) / 2 ^ 15, otherwise GainI2 = IBGain/2 ^ 15 .

The relationship between I2a before correction and I2b after correction is I2b=I2a+I2a*GainI2.

9.1.11 DC offset calibration register

Table 21 DC offset calibration register

DCIA	Addr:0x14H default:0000H		
W/R	Bit15	Bit14……Bit1	Bit0

DCIB	Addr:0x15H default:0000H		
W/R	Bit15	Bit14……Bit1	Bit0

DCU	Addr:0x16H default:0000H		
W/R	Bit15	Bit14……Bit1	Bit0

HLW8110/HLW8112 has three channels of DC offset calibration registers, which are used in metrology occasions without high-pass filters. The DC offset calibration register for each channel is 16 bits.

9.1.12 Voltage drop setting register

Table 22 Voltage drop setting register

SAGCYC	Addr:0x17H default:0000H		
W/R	Bit15	Bit14……Bit1	Bit0

SYSLVL	Addr:0x18H default:0000H		
W/R	Bit23	Bit22……Bit1	Bit0

Voltage sag characteristics are controlled by two registers: SAGCYC (unsigned number) and SAGLVL (unsigned number). These registers control the sag period and the sag voltage threshold respectively.

9.1.13 Threshold setting register

Table 23 Threshold setting register

OVLVL	Addr:0x19H default:FFFFH		
W/R	Bit15	Bit14……Bit1	Bit0

OIALVL	Addr:0x1AH default: FFFFH		
W/R	Bit15	Bit14……Bit1	Bit0

OIBLVL	Addr:0x1BH default: FFFFH		
W/R	Bit15	Bit14……Bit1	Bit0

OPLVL	Addr:0x1CH default: FFFFH		
W/R	Bit15	Bit14……Bit1	Bit0

OVLVL, OIALVL, OIBLVL and OPLVL are used to set voltage, current channel A, current channel B and active power overload threshold respectively (channel A and channel B share a set of overload threshold registers). The default value of registers is 0xFFFF; by default, this feature is disabled.

If HLW811X detects overcurrent, overvoltage and excessive power, OVIF/ROVIF,

OIAIF/ROIAIF, OIBIF/ROIBIF, OPIF/ROPIF will output the corresponding level state.

9.1.14 INT Function Output Selection Register

Table 24 INT Function Output Selection Register

INT Addr:0x1DH default：3210H		
Bit	Name	Description
15-12	NC	NC，default 0011
11-8	NC	NC，default 0010
7-4	P2sel	INT2 Pin Output Function Selection, See Table below
3-0	P1sel	INT1 Pin Output Function Selection, See Table below

Table 25 INT interrupt output function register

P1sel/P2sel	Description
0000	Output of Pulse PFA for Calibration of Electric Energy Meterin
0001	Output of Pulse PFB for Calibration of Electric Energy Meterin
0010	Leakage comparator indication signal
0011	Interrupt signal IRQ output (default is high level, if interrupt, set 0)
0100	Signal indication of power overload: only one of PA or PB can be selected
0101	Channel A Negative Power Indicator Signal
0110	Channel B Negative Power Indicator Signal
0111	Instantaneous value update interrupt output
1000	Average update interrupt output
1001	Voltage Channel Zero-Crossing Signal Output
1010	Current Channel A Zero-Crossing Signal Output
1011	Current Channel B Zero-Crossing Signal Output
1100	Overvoltage Indicator Signal Output of Voltage Channel
1101	Voltage Channel Undervoltage Indicating Signal Output
1110	Current Channel A Overcurrent Signal Indicating Output
1111	Current Channel B Overcurrent Signal Indicating Output

9.2 Metrological parameter register

9.2.1 Fast Active Power Pulse Counter

Table 26 PFCnt_PA/ PFCnt_PB

PFCnt_PA	Addr:0x20H default:0000H		
W/R	Bit15	14……1	Bit0

PFCnt_PB	Addr:0x21H default:0000H		
W/R	Bit15	14……1	Bit0

PFCnt_PB channel B fast active pulse count register; PFCnt_PA channel A fast active pulse count register;

In order to prevent power loss, the MCU reads and saves the PFCnt_PA and PFCnt_PB values of registers when the power is off, and then writes these values back to PFCnt_PA and PFCnt_PB when the next power is on.

When Prun = 0, PFCnt_PB and PFCnt_PB stop updating and remain unchanged; when Prun = 1:

When PFCnt_PB [15:1] equals the value of HFConst, PFB will have pulse output, and function register E_PB will add 1.

When PFCnt_PA [15:1] equals the value of HFConst, PFA will have pulse output and function register E_PA will add 1.

9.2.2 Phase Register

Table 27 Angle Register

Angle	Addr:0x22H defult:0000H		
R	Bit15	14……1	Bit0

Angle represents the angle between voltage channel and current channel A or between voltage channel and current channel B. When the line frequency is 50 Hz, the resolution is 0.0805 degrees; when the line frequency is 60 Hz, the resolution is 0.0965 degrees.

The linear frequency is 50Hz, and the formula for calculating phase angle is Angel = R*0.0805 degree.

The linear frequency is 60 Hz, and the formula for calculating phase angle is Angel = R*0.0965 degrees.

9.2.3 Voltage Frequency Register

Table 28 Ufreq Register

Ufreq	Addr:0x23H default:0000H		
R	Bit15	14……1	Bit0

It mainly measures the fundamental frequency and the measurement bandwidth is about

250Hz. The frequency value is a 16-bit unsigned number, and the parameter formatting formula is f=CLKI/8/Ufreq.

For example, if the system clock is CLKI = 3.579545MHz and Ufreq = 8948, the measured actual frequency is f = 3579545/8/8948 = 49.9908Hz.

The period of updating voltage and frequency measurements is 0.7s.

9.2.4 Current and Voltage RMS Register

Table 29 RmsIA/RmsIB/RmsU

RmsIA	Addr:0x24H default:000000H		
R	Bit23	22……1	Bit0

RmsIB	Addr:0x25H default:000000H		
R	Bit23	22……1	Bit0

RmsU	Addr:0x26H default:000000H		
R	Bit23	22……1	Bit0

RMS is a 24-bit signed number, the highest bit is 0 to represent the valid data, the highest bit is 1 hour reading to do zero processing; the frequency of parameter updates can be selected: 3.4 Hz, 6.8 Hz, 13.6 Hz, 27.2 Hz.

9.2.5 Power Factor Register

Table 30 PF

PF	Addr:0x27H default:000000H		
R	Bit23	Bit22……Bit1	Bit0
	Symbol	Data	Data

PF is a 24-bit signed decimal, the highest bit is the symbol bit, which is obtained by dividing the active power by the apparent power. Power factor = symbol bit *[(PF22*2^-1)+(PF21*2^-2)+...] When PF = 24'h7FFF, the power factor is 1.0; when PF = 24'h800000, the power factor is - 1.0; when PF = 24'h400000, the power factor is 0.5. The frequency of parameter updates is 3.4 Hz. The latent state is 24'h7FFF.

Formula: PF = | PF |/ 0x7FFFF;

9.2.6 Active Power Register

Table 31 Active Power Register

E_PA	Addr:0x28H default:000000H		
R	Bit23	22……1	Bit0

E_PB	Addr:0x29H default:000000H		
R	Bit23	Bit22……Bit1	Bit0

E_PA and E_PB are power energy registers, E_PA is channel A energy registers, E_PB is channel A energy registers. When 0 xFFFFFFFFFF overflows to 0 x000000, overflow flags PEAOIF and PEBOIF will be generated (see IF registers).

The power parameter is unsigned, the register value of E_PA represents the cumulative number of PFA pulses, and the register value of E_PB represents the cumulative number of PFB pulses. The minimum unit of register represents energy of 1/EckWh. EC is a pulse constant.

When EPA_CB=0, the E_PA register is a zero-clearing functional register, and when EPA_CB=1, the E_PA register is a zero-clearing functional register.

When EPB_CB=0, the E_PB register is a zero-clearing functional register, and when EPB_CB=1, the E_PB register is a zero-clearing functional register.

9.2.7 Average Power Register

Table 32 Average Power Register

PowerA	Addr:0x2CH default:00000000H		
R	Bit31	30……1	Bit0

PowerB	Addr:0x2DH default:00000000H		
R	Bit31	30……1	Bit0

PowerS	Addr:0x2EH default:00000000H		
R	Bit31	30……1	Bit0

Active power parameters PowerA/B and apparent power parameters PowerS are binary complement formats with 32 bits of data, the highest bit of which is the symbol bit.

PowerA is the average active power register of U channel and IA channel; PowerB is the average active power register of U channel and IB channel; PowerS is the average active power of voltage channel U and current channel A or the average active power of voltage channel U and current channel B, which is determined by channel_sel;

9.2.8 Meter Status Register

Table 33 EMU STATUS Register

EMU STATUS Register(EMUStatus) Addr:0x2FH Default：00EF3BH		
Bit	Name	Description
23-22	NC	NC
21	Channel_sel	Current channel chooses status identification bit. The default is 0. = 1. Current channel B is used to calculate phase angle, apparent power, power factor, instantaneous active power and instantaneous apparent power. = 0, indicating that current channel A is currently used to calculate phase angle, apparent power, power factor, instantaneous active power and instantaneous apparent power. When ADC2ON = 1, the bit is always 0.
20	NopldB	NopldB is set to 1 when the active power of channel B is less than the starting power (0060H); otherwise, it is set to 0.
19	NopldA	NopldA is set to 1 when the active power of channel A is less than the starting power (0060H); otherwise, it is set to 0
18	REVPB	Channel B reverse active power indicator identification signal. When the active power is detected, the signal is 1. When the positive active power is detected again, the signal is 0. This value is updated when the PFB pulse occurs.
17	REVPA	Channel A reverse active power indicator identification signal. When the active power is detected, the signal is 1. When the positive active power is detected again, the signal is 0. This value is updated when the PFA pulse occurs.
16	ChksumBusy	Calibration Calculating State Register for Calibration Data = 0, indicating that the data checking and calculation of the calibration table have been completed, and the checking value is available. = 1, It means that the data checking and calculation of the calibration table are not completed and the checking value is not available.
15—0	Chksum	CheckSum output

EMUStatus [15:0] is a special register provided by HLW811X to store the 16-bit checksum of the calibration parameter configuration register. The external MCU can detect

this register to monitor whether the calibration data is disordered.

The algorithm of checksum is double-byte accumulation and reverse. For a single-byte register, it is expanded to double-byte and then accumulated. The extended byte is 00H.

The register address of HLW811X participating in checking and calculation is 00H-1FH, and the checksum calculated according to the default value of HLW811X is 0xB32E.

In the following three cases, a check and calculation is restarted: system reset, write operation occurs in a register of 00H-10H, write operation occurs in a register of 00H-1FH, read operation occurs in an EMUStatus register. Two system clock cycles are required for a checksum calculation.

9.3 Peak Register

Table 34 PeakIA/ PeakIB/ PeakU

PeakIA	Addr:0x30H default:000000H		
R	Bit23	Bit22……Bit1	Bit0

Peak Register of Current Channel A, Clear After Reading.

PeakIB	Addr:0x31H default:000000H		
R	Bit23	Bit22……Bit1	Bit0

Peak Register of Current Channel B, Clear After Reading.

PeakU	Addr:0x32H Default:000000H		
R	Bit23	Bit22……Bit1	Bit0

Peak Register of Current Channel U, Clear After Reading.

9.4 Instantaneous Value and Waveform Register

9.4.1 Instantaneous value register

Table 35 InstanIA/ InstanIB/ InstanU

InstanIA	Addr:0x33H default:000000H		
R	Bit23	Bit22……Bit1	Bit0

Current channel A RMS instantaneous value, update frequency is 6991Hz.

InstanIB	Addr:0x34H default:000000H		
R	Bit23	Bit22……Bit1	Bit0

Current channel B RMS instantaneous value, update frequency is 6991Hz.

InstanU	Addr:0x35H default:000000H		
R	Bit23	Bit22……Bit1	Bit0

Current channel U RMS instantaneous value, update frequency is 6991Hz.

PowerP	Addr:0x3CH default:00000000H		
R	Bit31	Bit30……Bit1	Bit0

Active power instantaneous value, update frequency is 6991Hz.

PowerS	Addr:0x3DH default:00000000H		
R	Bit31	Bit30……Bit1	Bit0

Regarding the instantaneous power value, the update frequency is 6991Hz.

9.4.2 Waveform Register

Table 36 Waveform Register

WaveIA	Addr:0x36H default:000000H		
R	Bit23	Bit22……Bit1	Bit0

Current channel A RMS instantaneous value, the highest bit is the symbol bit, the update frequency is 6991Hz

WaveIB	Addr:0x37H default:000000H		
R	Bit23	Bit22……Bit1	Bit0

Current channel B RMS instantaneous value, the highest bit is the symbol bit, the update frequency is 6991Hz

WaveU	Addr:0x38H default:000000H		
R	Bit23	Bit22……Bit1	Bit0

Current channel U RMS instantaneous value, the highest bit is the symbol bit, the update frequency is 6991Hz

9.5 Interrupt status register

9.5.1 Interrupt Configuration and Allowed Register IE

The IRQ_N (INT1/INT2) pin output is low when the interrupt allowable bit is configured to be 1 and the interrupt occurs. Write Protection Register. Write enable should be opened before configuring the register.

Table 37 Interrupt Enable Register(IE)

Interrupt Enable Register(IE) Addr:0x40H default：0000H		
Bit	Name	Description

15	LeakageIE	Leakage interruption enable
14	ZX_UIE	Voltage zero-crossing interruption enable
13	ZX_IBIE	Current A Zero-crossing Interruption Enable
12	ZX_IAIE	Current B Zero-crossing Interruption Enable
11	SAGIE	Voltage Zero-crossing Interruption Enable
10	OPIE	Power overload enable
9	OVIE	Voltage Overvoltage Interruption Enablae
8	OIBIE	Current B Overcurrent Interruption Enable
7	OIAIE	Current A Overcurrent Interruption Enable
6	INSTANIE	Instantaneous interruption enablement
5	Retain	
4	PEBOIE	Channel B Active Power Register Overflow Interrupt Enablation
3	PEAOIE	Channel A Active Power Register Overflow Interrupt Enablation
2	PFBIE	PFB interrupt enable
1	PFAIE	PFB interrupt enable
0	DUPDIE	Average data update interrupt enable

9.5.2 Interrupt Status Register IF

Table 38 IF Interrupt Enable Register

Interrupt Enable Register(IF) Addr:0x41H default：0000H		
Bit	Name	Description
15	LeakageIF	=0，No leakage interruption occurred =1，Leakage interruption
14	ZX_UIF	=0，No zero-crossing interruption occurred =1，Voltage zero-crossing interruption
13	ZX_IBIF	=0，No current B zero-crossing interruption occurred =1，Current B zero-crossing interruption
12	ZX_IAIF	=0，No current A zero-crossing interruption occurred =1，Current A zero-crossing interruption occurs
11	SAGIF	=0，No undervoltage interruption occurred =1，Voltage undervoltage interruption
10	OPIF	=0，No power overload interruption occurred =1，Power overload interruption
9	OVIF	=0，No voltage overvoltage interruption occurred =1，Voltage overvoltage interruption
8	OIBIF	=0，No current B over-current interruption occurred =1， Current B Overcurrent Interruption
7	OIAIF	=0， No current A overcurrent interruption occurred

		=1， Current A Overcurrent Interruption
6	INSTANIF	INSTANIF=0，No instantaneous value update event occurred； INSTANIF=1，An instantaneous value update event occurs；
5	NC	NC
4	PEBOIF	PEBOIF=0: No active power register overflow event occurred in channel B; PEBOIF=1: Active Power Register Overflow Event in Channel B;
3	PEAOIF	PEAOIF=0: No active power register overflow event occurred in channel A; PEAOIF=1: Active Power Register Overflow Event in Channel A;
2	PFBIF	PBFIF=0: No PFB pulse output event occurred; PBFIF=1: No PFB pulse output event occurred;
1	PFBIF	PAFIF=0: No PFA pulse output event occurred; PAFIF=1: PFA Pulse Output Event Occurs;
0	DUPDIF	DUPDIF =0: No data update event occurred; DUPDIF =1: Data Update Event Occurs.

IF is suitable for SPI interface and UART interface. When an interrupt event occurs, the hardware will set the corresponding interrupt flag at 1.

The generation of IF interrupt flag is controlled by the interrupt admission register IE, and the corresponding interrupt status register flag bit will be updated after setting IE.

IF is a read-only register and clears after reading.

9.5.3 RIF Reset interrupt status register RIF

Table 39 Reset Interrupt Flag Register

Reset Interrupt Flag Register Addr:0x42H default：0000H		
Bit	Name	Description
15	RleakageIF	=0，No leakage interruption occurred =1，Leakage interruption
14	RZX_UIF	=0，No zero-crossing interruption occurred =1，Voltage zero-crossing interruption
13	RZX_IBIF	=0，No current B zero-crossing interruption occurred =1，Current B zero-crossing interruption
12	RZX_IAIF	=0，No current A zero-crossing interruption occurred =1，Current A zero-crossing interruption occurs
11	RSAGIF	=0，No undervoltage interruption occurred =1，Voltage undervoltage interruption
10	ROPIF	=0，No power overload interruption occurred =1，Power overload interruption
9	ROVIF	=0，No voltage overvoltage interruption occurred

		=1，Voltage overvoltage interruption
8	ROIBIF	=0，No current B over-current interruption occurred =1，Current B Overcurrent Interruption
7	ROIAIF	=0，No current A overcurrent interruption occurred =1，Current A Overcurrent Interruption
6	RINSTANIF	=0，No instantaneous value update event occurred =1，Instantaneous value update event
5	Retain	
4	RPEBOIF	=0: No active power register overflow event occurred in channel B =1:Active Power Register Overflow Event in Channel B
3	RPEAOIF	=0:No active power register overflow event occurred in channel A; =1:Active Power Register Overflow Event in Channel A;
2	RPFBIF	=0:No PFB pulse output event occurred; =1: PFB Pulse Output Event Occurs
1	RPFAIF	=0: No PFA pulse output event occurred; =1:PFA Pulse Output Event Occurs;
0	RDUPDIF	=0: No data update event occurred =1: Data Update Event Occurs

For SPI and UART, the bit definition of RIF is the same as that of IF. When an interrupt event occurs, the corresponding interrupt flag is set to 1. Read RIF to clear IF and RIF registers at the same time. RIF is designed to receive new interrupts while reading the interrupt flag register in SPI/UART.

9.6 System Status Register

9.6.1 System Status Register

Table 40 Systatus

System Status Register (SysStatus)		Addr： 0x43H	Only Read
Bit	Name	Description	
7	Retain	Read 0	
6	clksel	Clock Source Indicating Signal in Chip System =1，Chips are using internal crystal oscillators =0，Chips are using external crystal oscillators	
5	Retain		
4	WREN	Write enable flag: = 1 allows writing to write to write-protected registers; = 0 does not allow writing to write to write-protected registers	
3	Retain	Read 0	

2	Retain	Read 0
1	Retain	Read 0
0	RST	Reset sign. When the external RST_N pin, the power-on reset end and the software global reset, the position 1 can be cleared after reading, and can be used for the data request of the calibration table after reset.

9.6.2 SPISPI Read Check Register RDATA

Table 41 Read Check Register RDATA

RDATA	Addr:0x44H default:00000000H		
R	Bit31	Bit30……Bit1	Bit0

The Rdata register holds the last read 4 bytes of data and can be used to verify the read data.

9.6.3 SPI Write Check Register WDATA

Table 42 SPI Write Check Register WDATA

WDATA	Addr:0x45H default:0000H		
R	Bit15	Bit`4……Bit1	Bit0

The Wdata register holds the last written 2-byte data and can be used for verification when writing data.

9.6.4 Coefficient Register and Standby Register

Table 43 Coefficient Register

RmsIAC	Addr:0x70H default:FFFFH		
RmsIBC	Addr:0x71H default:FFFFH		
RmsUC	Addr:0x72H default:FFFFH		
PowerPAC	Addr:0x73H default:FFFFH		
PowerPBC	Addr:0x74H default:FFFFH		
PowerSC	Addr:0x75H default:FFFFH		
EnergyAC	Addr:0x76H default:FFFFH		
EnergyBC	Addr:0x77H default:FFFFH		
CheckSum	Addr:0x6fH default:FFFFH		
W/R	Bit15	Bit14……Bit1	Bit0

Uncalibrated HLW8110/HLW8112, the default value of conversion coefficient is 0 xffff. When calibrated out of the factory, the coefficient value will change. Thus, these coefficients can be used to calculate the power parameters of the calibration-free formula.

The RmsxxC register stores a 16-bit unsigned number of RMS conversion coefficients. Assuming that the external current is 5A, RmsIAC = 5000/RmsIA*2^23. When the current is displayed, the value of RmsIAC can be read out and calculated: current value = RmsIA*RmsIAC/2^23.

PowerxxC registers store active power or apparent power conversion coefficients, which are 16-bit unsigned numbers.

The value of OTP loaded by coefficient register and standby register; Check sum = ~(FFFFH + RmsIAC +..... + EnergyBC), Take two bytes lower.

10 Calibration-free calculation method

Table 44 Calibration-free PGA settings

VDD	5V	
Current A	PGA=16 ,Input Single:5mV、	Current IRMS 5A
Current B	PGA=16, Input Single 5mV	Current IRMS 5A
Voltage u	PGA=1, Input Single 200mV	Votltage URms 200V
Active Power		Active Power 1000W
Apparent Power		Apparent Power 1000W

Note: The coefficient calculation of the chip is realized by directly applying AC voltage signal outside, without considering the influence of the errors of resistors (current channel manganese-copper resistance, voltage channel divider resistance) and other peripherals. The error of the coefficient calculation is within (+1%).

When the sampling resistance of current channel is K1*1mΩ (K1 is the magnification/reduction multiple, for example, manganese copper is actually 2mΩ, K1=2; manganese copper is actually 0.5mΩ, K1=0.5); the voltage dividing resistance ratio is K2*1KΩ/1M (K2 is the magnification/reduction multiple, for example, the voltage dividing resistance ratio is actually 2K/1MΩ, K2=2; and the voltage dividing resistance ratio is actually 0.82KΩ/1M, K2=0.82;), the calculation can be based on the following formula:

RMS calculation method:

$$\mathrm{Irms} = \frac{\mathrm{RmsIXX} * \mathrm{RmsIXXC}}{\mathrm{K1} * 2^{23}}$$

$$\mathrm{Urms} = \frac{\mathrm{RmsUXX} * \mathrm{RmsUXXC}}{\mathrm{K2} * 2^{22}}$$

RmsXX is the current/voltage RMS register value and RmsXXC is the current/voltage RMS coefficient register value.

Current RMS is calculated in mA (for example, 5000.1, representing 5.0001A) and voltage RMS is calculated in 10mV (for example, 22008.1, representing 220.081V).

Active/apparent power calculation method：

$$\text{Active Power/Apparent Power} = \frac{\text{PowerXX} * \text{PowerXXC}}{\text{K1} * \text{K2} * 2^{31}}$$

PowerXX is the active power/apparent power register value, RmsXXC is the current/voltage RMS coefficient register value.

Active power/apparent power is calculated in W (e.g. 1100.1, representing 1100.1W).

Energry Calculation formula：

$$\text{Energry} = \frac{\text{EnergyXX}*\text{EnergyXXC}*\text{HFconst}}{\text{K1}*\text{K2}*2^{29}*4096}$$

EnergyXX is the energy pulse register value and EnergyXXC is the energy pulse calibration coefficient register value.

The unit for calculating electric energy is KW*h (e.g. 2.101, representing 2.101 kWh).

11 Calibration method

11.1 Summary

HLW8110/HLW8112 can realize software calibration. After calibration, the active power accuracy can reach 0.5s. The calibration of HLW8110/HLW8112 includes:

- Adjustable HFConst
- Provide phase calibration of A/B channel
- Current Gain Calibration for B Channel
- Active Gain Calibration for A/B Channels
- Active Offset Calibration Providing A/B Channel
- Offset Calibration Provides Valid Value of A/B Channel
- Provide gain calibration and Offset calibration for apparent power
- Provide automatic calibration function of calibration data

11.2 Calibration process and parameter calculation

Standard watt-hour meters must be provided when calibrating single-phase liquid crystal

meters designed by HLW8110/HLW8112. When calibrating a standard watt-hour meter, PFA/PFB with functional pulses can be directly connected to the standard watt-hour meter by optocoupler, and then HLW8110/HLW8112 can be calibrated according to the error readings of the standard watt-hour meter.

Calibration process

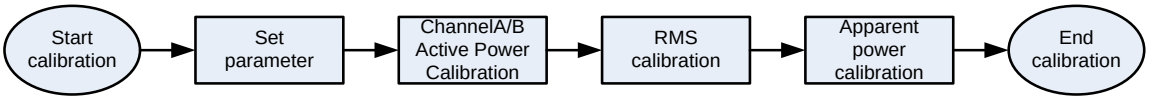


Figure 25 Calibration process

11.3 Parameter set

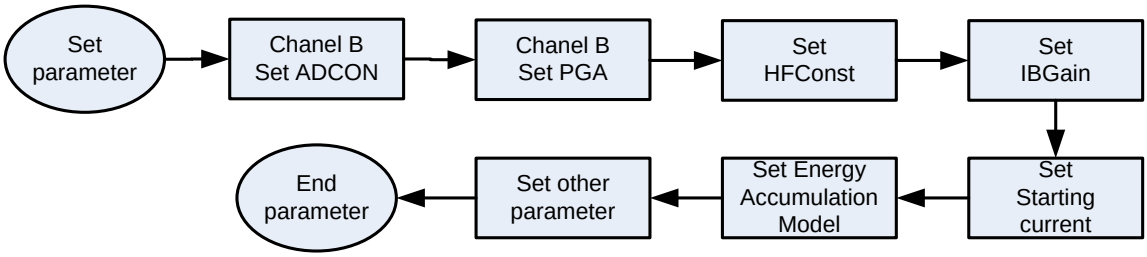


Figure 26 Parameter Setting Flow

HFConst parameter calculation:

HFConst formula (calculated by the current of channel A):

$$HFConst = 23.2*10\text{^}11*\frac{Vu*Vi}{EC*Un*Ib}$$

Vu：When rated voltage is input, the voltage of voltage channel (pin voltage * amplification multiple: 1, 2, 4, 8, 16);

Vi： When rated current is input, the voltage of current channel (pin voltage * amplification multiple: 1, 2, 4, 8, 16);

Un： Rated input voltage;

Ib： Rated input current;

EC： Pulse constant

IBGain's calculations:

IBGain = (IA-IB) / IB.

If IBGain is greater than or equal to 0, IBGain = INT [IBGain x 2^15];

Otherwise, if IBGain < 0, IBGain = INT [2^16 + IBGain * 2^15];

IA: Current RMS of Current Channel A (RmsIA register value);

IB: Current RMS of Current Channel B (RmsIB register value).

11.4 Active power calibration

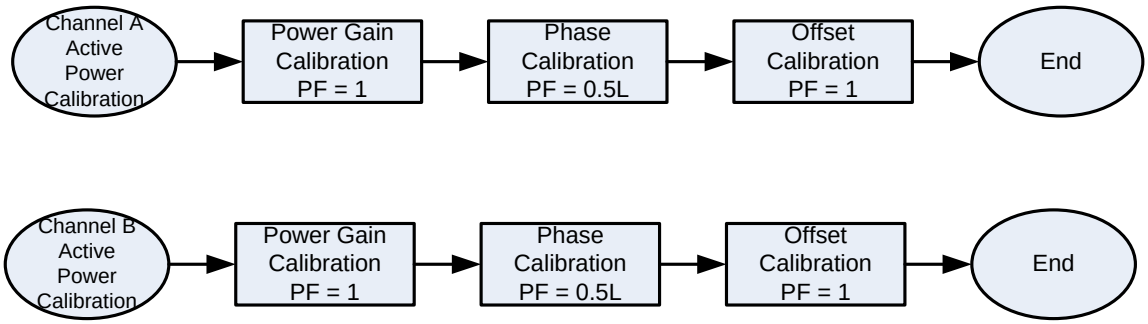


Figure 27 Active Power Calibration Process

1. A-channel power gain calibration can be achieved by configuring PAGain registers. The calculation method of PAGain is as follows:

If the reading error of the standard table on channel A 100% Ib and PF = 1 is err: PAGain=-err/(1+err).

If PAGain is greater than or equal to 0, then PAGain = INT [PAGain * 2^15]; Otherwise, if PAGain < 0, PAGain = INT [2^16 + PAGain * 2^15];

B-channel power gain calibration can be achieved by configuring PBGain registers, which is the same as PAGain.

2. Calculating method of A/B channel phase calibration register:

If the readout error of the standard table is err on A/B channel, 100% Ib, PF=0.5L, the phase compensation formula is:

θ= arcsin (-err/sqrt(3)*180/3.14159

Orθ= arccos ((err+1)/2)*180/3.14159-60 degrees

For 50Hz, PhaseA/B has a 0.02 degree/LSB relationship, while PhaseA/B has a 0.02 degree/LSB relationship.

Ifθ>= 0, PhaseA/B = INT [θ/0.02].

Ifθ< 0, PhaseA/B = INT [2^8+θ/0.02].

3. Active Offset calibration is based on the integration of energy shadows from larger external noise (PCB noise, transformer noise, etc.).

In the case of small signal accuracy, it is an effective means to improve the active precision of small signal. If the external noise has little influence on the active accuracy of small signal, this step can be neglected. If the reading error is err and the value of PowerA register is PA when the standard meter applies Un, channel A 5% Ib and PF = 1 to the watt-hour meter, then the calculation process of PAOS register is as follows:

PAOS = INT [-(PA*err)];

PBOS registers are computed in the same way.

11.5 RMS calibration

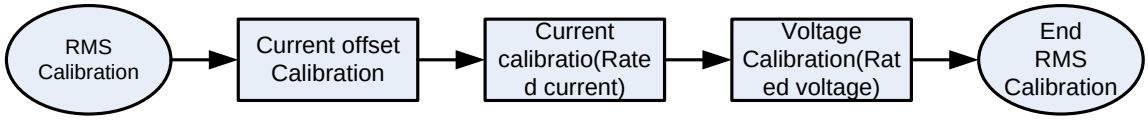


Figure 28 Valid Value Calibration Process

1. Current Offset Calibration Can Improve the Precision of Small Signal Current RMS

RmsIAOS Register Computing Process：

1) Configure standard table, make U = Un, current channel input Vi = 0;

2) Wait for DUPDIF ID bit update (refresh around 3.4 Hz per second);

3)MCU takes RmsIA register value for temporary storage;

4) Step 2 and 3 were repeated 11 times, the first data was not needed, and the last 10 data were averaged to Iave [23:0].

5) Iave is reversed bit by bit (including symbol bit) plus 1. Bit15 of RmsIAOS register is filled with symbol bit, and RmsIAOS is obtained by filling Bit14-Bit0 with RmsIAOS Bit14-Bit0.

6) Valid Value Offset Calibration End

The RmsIBOS calibration formula and the RmsIAOS register calculation process are the same.

2. After the current Offset is calibrated, the A/B channel current conversion coefficient KiA/KiB and voltage conversion coefficient Ku are calibrated. This step is completed by MCU. The calculation process is as follows:

If the RmsIA register reading under rated current Ib is RmsIAreg, then KiA=Ib/RmsIAreg.

iA is the ratio of the rated input value to the corresponding register.

The calculation process of channel B conversion coefficient KiB and voltage conversion coefficient Ku is the same.

11.6 Apparent power calibration

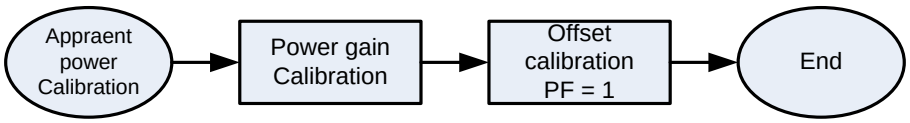


Figure 29Arrarent power calibration

1. The apparent power gain calibration can be achieved by configuring PSGain registers. The calculation method of PSGain is as follows:

If the channel of energy measurement is A channel, the average power register value of reading A channel is PowerPA when the standard meter applies Un, A channel 100% Ib, PF = 1. The average power register value is PowerS:

PSGain=(PowerPA-PowerS)/ PowerS。

If PSGain ≥0，PSGain =INT[PSGain ×215]；

If PSGain ＜0，PSGain =INT[216 +PSGain ×215]；

2. Visual Offset Calibration helps to improve the accuracy of power factor for small signals

If the channel of energy measurement is A channel, the average active power register value of reading A channel is PowerPA and the average power register value is PowerS when the standard meter applies Un, 5% Ib and PF=1 to the watt-hour meter, then the calculation process of PSOS register value is as follows:

PSOS = INT[PowerPA-PowerS]；

11.7 Example

Suppose a 220V (Un) and 10A (Ib) rated input is designed. The pulse constant is 1200imp/kWh (EC). A channel current uses 250uΩ, channel A analog channel gain is 16 times, B channel current sampling uses current transformer, B channel gain is 1 times, voltage sampling uses resistance voltage dividing input, and analog channel gain is 16 times. The Pin value of the chip is 0.16V.

1:Computing HFConst

Vu=0.16V，Vi=10×0.00025×16=0.040V，EC=1200imp/kWh，Un=220v，Ib=10A。hfconst＝int[23.196×vu×vi×1011/（ec×un×ib）]=5623=15f7h，hfconst 15f7h，hfconst-hfconst，hfconst-hfconst。

2：Active power Calibration of Channel A

2.1 A Channel Power Gain Calibration

The output power factor of 220V 10A on the power source is 1.0, and the display error of the standard meter is 1.2%.

PAGain=-0.012/(1+0.012)=-0.01186,

PAGain<0, PAGain=INT[216+PAGain*215]=-0.01186*215+216=0xFE7BH, FE7BH is written into PAGain register to complete channel A gain calibration.

2.2 A Channel Phase Calibration

After the resistance gain is calibrated, the power factor is changed to 0.5L, and the error

shown by the standard table is -0.4%, thenθ> 0, PhaseA = INT [θ/0.02]= (arcsin (-(-0.004)/sqrt (3))))/0.02= 7, input 07H to the PhaseA register to complete the A channel phase calibration; if the error shown by the standard table is -0.4%,θ> 0, PhaseA = INT [theta/0.02]= (sin) (-0.004)/arcs register, then theta > 0.4. QRT (3)/0.02=-7, input (2 ^ 8-7-96) = 99H to PhaseA register when Phase_sel=0, input (2 ^ 8-7) = F9H to PhaseA register when Phase_sel=1;

2.3 A Channel Offset Calibration

If the standard meter applies Un, A channel 5% Ib, PF = 1 to the watt-hour meter, the reading error is err = 0.3%, and the value of PowerA register is PA = 000F5AB7H (the average value of 16 consecutive reads and the refresh frequency of PowerA is about 3.4Hz), then the value of PAOS register is PAOS = INT [-(000F5AB7H * 0.3%)]= F436H.

Active calibration of channel B is similar to channel A.

3：RMS calibration

The chip provides a current RMS offset calibration register. Under the condition that the current input is zero, the read current RMS register is 268H (average value can be read several times), the reverse plus 1 is FFFD98, the symbol bit is filled into Bit15 of RmsIAOS register, and the Bit14-Bit0 is filled into PAOS Bit14-Bit0 to get FD98H, which is written into RmsIAOS register. A channel RMS calibration is completed.

B channel RMS calibration is similar to A channel.

11.8 Apparent power calibration

11.8.1 Apparent power calibration

Assuming that the channel of energy measurement is A channel, the average active power register value of read-out A channel is PowerPA = 00AF389AH, and the average power register value is PowerS = 00AE04D4H when the standard meter imposes Un, A channel 100% Ib, PF = 1 on the watt-hour meter, then the calculation process of PSGain register value is as follows:

PSGain= (PowerPA-PowerS)/ PowerS = 0.691%;

PSGain = INT [PSGain * 2 ^ 15] = 226 = 00E2H;

11.8.2 Apparent Power Offset Calibration

Assuming that the channel of energy measurement is A channel, the average active power register value of read-out A channel is PowerPA = 0008C2D4H, and the average power register value is PowerS = 0008C1D7H when the standard meter applies Un, A channel 5% Ib, PF = 1 to the watt-hour meter, then the calculation process of PSOS register

value is as follows:

PSOS = INT [PowerPA - PowerS] = 253 = 00FDH;

12 Communication protocol

12.1 SPI communication

If the SPEN pin of HLW8112 is connected to high level, HLW8112 is the SPI communication mode.

12.1.1 SPICommand format

SPI is a four-wire system: SCSN, SDI, SDO and SCLK, including a read register RDATA and a write register WDATA. All data transmission errors are synchronized with SLCK. HLW8112 outputs data from SDO pins at the rising edge and reads data from SDI pins at the falling edge. During the low period of SCSN, the register can be read and written continuously. During SPI operation, reset the SPI module (the minimum SPI rate is 109.25Hz) if the two SCLK rising edges exceed 9.15ms (2 ^ 15 of the system clock).

The SPI command register is an 8 bit wide register. For the read-write operation, the bit7 of the command register is used to determine whether the type of data transmission operation is read operation or write operation, and the bit6-0 of the command register is the address of the read-write register. For special command operations, bit7-0 of the command register is fixed to 0xEA.

Command	Command register	Data	Description
Read command	{0[bit7],REG_ADR[bit6:bit0]}	RDATA	Read data from registers with REG_ADR [6:0] The highest bit is 0, which means reading data to registers.
Write command	{1[bit7],REG_ADR[bit6:bit0]}	WDATA	Write data to registers with REG_ADR [6:0] The highest bit is 1, which means writing data to registers.
Write enable order	0xEA	0xE5	Enable write operation
Write Protection Command	0xEA	0xDC	Close write operation
Channel A	0xEA	0x5A	Current channel A setting command

select			specifies the current signal used to calculate apparent power, power factor, phase angle, instantaneous apparent power and active power overload as channel A
Channel B select	0xEA	0xA5	Current channel B setting command specifies the current signal used to calculate apparent power, power factor, phase angle, instantaneous apparent power and active power overload as channel B
Reset instruct	0xEA	0x96	Reset instruct, chip reset after receiving instruction

表 1 HLW8112 SPI command list

12.1.2 Switch character

AVDD = DVDD = 5V±5%;AGND = DGND =0V

Logic Levels:Logic0 = 0V,Logic1 = DVDD

Table 45 Switch Character Table

parameter	Symbol	Min	Typicl	Max	Unit
Rise time	Trise	-	0.05	1.0	uS
Fall time(note 1)	Tfall	-	0.05	1.0	uS
start-up					
Start-up time of crystal oscillator 3.579545MHZ(note 2)	Tost	0.11	-	60	ms
Time Character of Serial Port					
Serial clock frequency	SCLK	0.11	-	MCLK/4	KHz
Time of data bytes	t1	0.5	-	-	Tsclk
The time between the descending edge of SCLK and the ascending edge of SCSN	t2	0.5	-	-	Tsclk

Note: 1. The parameter test uses two points of 10% and 90% waveform, and the output load is 50PF.

2. The starting time of the oscillator varies with the crystal parameters, which are invalid when external clocks are used.

12.1.3 SPI interface timing

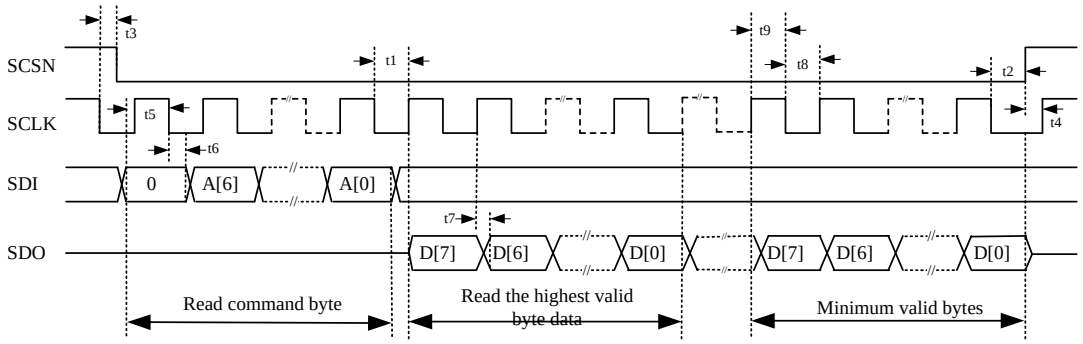


Figure 30 SPI Reading Interface Sequence Diagram

Working Process：

After the switchboard is valid in SCSN, it writes command bytes through SPI. After receiving the read command from the switchboard, the data is output bitwise from the SDO pin at the rising edge of SCSN. Be careful:

1、In bytes, high bits are in the front and low bits are in the back;

2、Multi-byte registers, which first output high-byte content and then transmit low-byte content;

3、The host in SCLK rises along oblique command bytes, and the slave in SCLK rises along the output data from SDO.

4、The time T1 of data byte is greater than or equal to half SCLK time.

5、The last byte of LSB transmission is completed, and the SCSN data transmission is completed from low to high. The time T2 between the descending edge of SCLK and the ascending edge of SCLN is greater than or equal to half of the SCLK cycle.

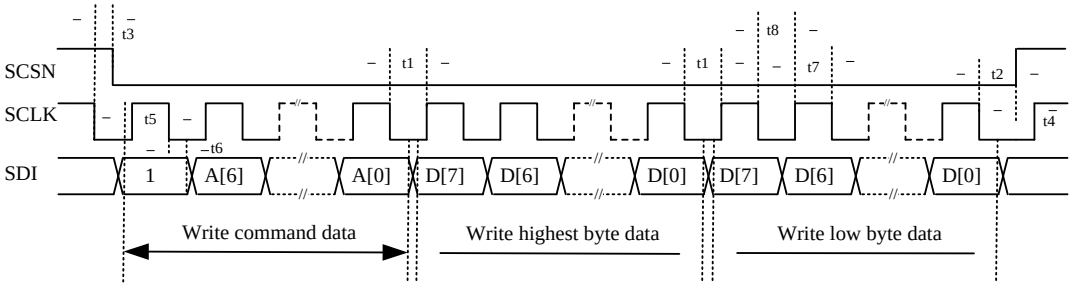


Figure 31 SPI Write Interface Sequence Diagram

Wrok process：

After the host is valid in SCSN, it first writes command bytes through SPI, and then writes data bytes. Be careful

1、Transmit in bytes, with high bits ahead and low bits behind.

2、Multi-byte registers, which transfer high-byte content first, and then low-byte content

3、The host writes data on the ascending edge of SCLK, and the slave reads data on the descending edge of SCLK.

4、Time T1 between data bytes should be greater than or equal to half of the SCLK cycle

5、The last byte of LSB transmission is completed, and the SCSN data transmission is completed from low to high. The time T2 between the descending edge of SCLK and the ascending edge of SCLN is greater than or equal to half of the SCLK cycle.

Note: Write-enabled commands must be written between write operations in registers with write protection.

The timing relationship of calibration pulse PF is shown in Fig. 22.

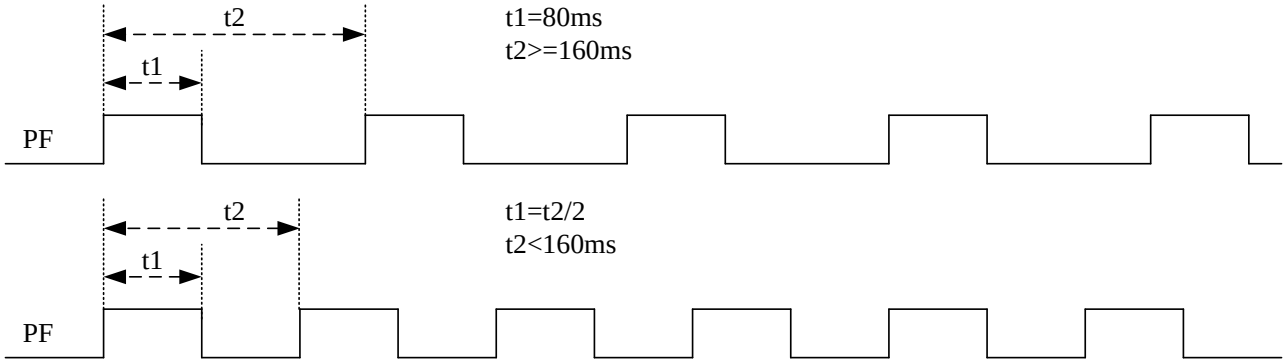


Figure 32 Output Port PF Sequence Diagram

As shown in Figure 27, when the PF pulse period is greater than or equal to 160ms, the PF pulse width is fixed at 80 ms, and when the PF pulse period is less than 160ms, the PF output is 50% duty cycle.

12.2 UART communication

12.2.1 UART communication format

Working in slave mode, half-duplex communication, 9-bit UART (including parity bits), conforming to standard UART protocol

When the SPEN pin connection of HLW8110/HLW8112 chip is low and the internal serial communication port is transferred to UART mode, SDO/TX is converted to transmit and output TX, SDI/RX is converted to receive input RX, SCLK and SCSN control the baud rate of UART, as shown in the table below.

SPIEN	SCLK	SCSN	Description
1	X	X	SPI communication
0	1	1	UART baud rate :38400
0	0	1	UART baud rate :19200
0	1	0	UART baud rate :9600(HLW8110 fixed this baud rate)

The UART communication format of HLW8112/HLW8110 is as follows:

0xA5	Command CMD	DataH MSB	……	……	DataL LSB	check Cdata

UART command register is the same as SPI, and it's also an 8 bit wide register. For the read-write operation, the command register bit7 is used to determine whether the type of data transmission operation is read operation or write operation. For special command operations, bit7-0 of the command register is fixed to 0xEA.

UART data transmission of HLW8112/HLW8110: Read operation is sent by slave and write operation is sent by host. If the register address corresponds to a multi-byte register, the highest valid byte is passed first.

UART data verification mode of HLW8112/HLW8110: read operation is sent by slave and write operation is sent by host. Calculating methods of calibration data are as follows:

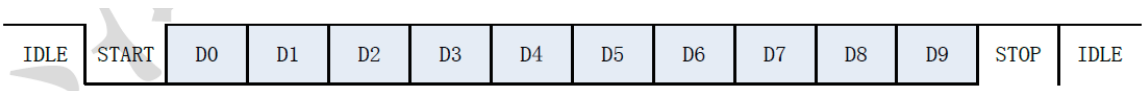
Check data Cdata [7:0] = A5 + CMD [7:0] + DATAn [7:0] +... + DATA1 [7:0], which adds CMD and data, discards carry, and the final result is reversed bit by bit.

Command Name	Command Register	Data	**Description**
Read command	{0[bit7],REG_ADR[bit6:bit0]}	RDATA	Read data from registers with REG_ADR [6:0] The highest bit is 0, which means reading data to registers.
Write command	{1[bit7],REG_ADR[bit6:bit0]}	WDATA	Write data from registers with REG_ADR [6:0] The highest bit is 0, which means

			Writing data to registers.
Write enable order	0xEA	0xE5	Enable write operation
Write Protection Command	0xEA	0xDC	Close write operation
Channel A select	0xEA	0x5A	Current channel A setting command specifies the current signal used to calculate apparent power, power factor, phase angle, instantaneous apparent power and active power overload as channel A
Channel B select	0xEA	0xA5	Current channel B setting command specifies the current signal used to calculate apparent power, power factor, phase angle, instantaneous apparent power and active power overload as channel B
Reset instruct	0xEA	0x96	Reset instruct, chip reset after receiving instruction

12.2.2 UART frame format timing

The UART communication of HLW8110/HLW8112 transmits data in 11 bits: 1 start bit, 8 data bits (low bit first), 1 parity bit (9 data bit) and 1 stop bit.



12.2.3 UART Write Operation

Writing is initiated by the host, which sends command bytes. If it is writing commands, the slave continues to receive digital bytes and checksum bytes sent by the host in turn.

0xA5	Command CMD	DataH MSB	……	……	DataL LSB	Check Cdata

Note:

1. The byte sender calculates and sends the check bits, and the byte receiver judges whether the byte transfer is valid or not based on the check bits.
Fruit byte error, and subsequent bytes are considered the beginning of the new frame;
2. Multi-byte registers transmit high-byte content first, and then low-byte content.
3. The time between bytes sent by the host is controlled by the host without restriction.
4. The time between complete command communication is controlled by the host without restriction.
5. Registers with write protection should write write write enabling commands before writing operations.
6. The host calculates and sends the checksum, and the slave judges whether the frame transmission is successful or not according to the checksum.

For example, when writing data 1234H to HFCST address 02H, UART data is sent as follows:

1. First frame transmission: 0xA5;
2. Second frame transmission: 0x82;
3. Third frame transmission: 0x12;
4. Fourth frame transmission: 0x34;
5. Fifth frame transmission: 0x92; 0x92= ~[A5+82+12+34], take 8 bit lower data;

12.2.4 UART Read Operation

The read operation is initiated by the host, which sends the read command bytes first, and then HLW8112/HLW8110 sends the read data bytes, read checksum bytes by TX. As shown in the following figure:

0xA5	Command CMD	DataH MSB	……	……	DataL LSB	check Cdata

Note：

1. The byte sender calculates and sends the check bits, and the byte receiver judges whether the byte transfer is valid or not based on the check bits. The byte receiver considers the current frame error and ends it.
2. Multi-byte registers transmit high-byte content first, and then low-byte content.
3. The time between the bytes sent by the host is controlled by the host without restriction.
4. The switching time between read command and data dataout is controlled by HLW8112/HLW8110: T/2 (T is the transmission time per bit);

5. The time between data bytes sent by HLW8112/HLW8110 is controlled by HLW8112/HLW8110: T (the transmission time per bit);
6. The time between complete command communication is controlled by the host without restriction.
7. The host calculates and sends checksum to judge whether HLW8112/HLW8110 frame transmission is successful or not.
For example, read the HFCST data with address 02H and send it as follows:
1. The first frame sends 9 bits of data: 8'hA5 + check bits;
2. The second frame sends 9 bits of data: 8'h02 + check bits;
3. The third frame receives 9 bits of data (high 8 bits + check bits of HFCONST); judges whether the received check bits are correct or not.
4. The fourth frame receives 9 bits of data (low 8 bits of HFCONST); judges whether the received check bits are correct or not.
5. The fifth frame receives the check data and judges whether the received check data is correct.

13 Package

13.1 HLW8110 package

HLW8110 is encapsulated with SOP8. The encapsulation information is shown as follows:

Label \ Size	Min （mm）	Max （mm）	Label \ Size	Min （mm）	Max （mm）
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20TYP	
A2	1.27TYP		D	1.05TYP	
A3	0.41TYP		D1	0.40	0.60
B	5.80	6.20	R1	0.07TYP	
B1	3.80	4.00	R2	0.07TYP	
B2	5.0TYP		θ1	17°TYP	
C	1.30	1.50	θ2	13°TYP	
C1	0.55	0.65	θ3	4°TYP	
C2	0.55	0.65	θ4	12°TYP	

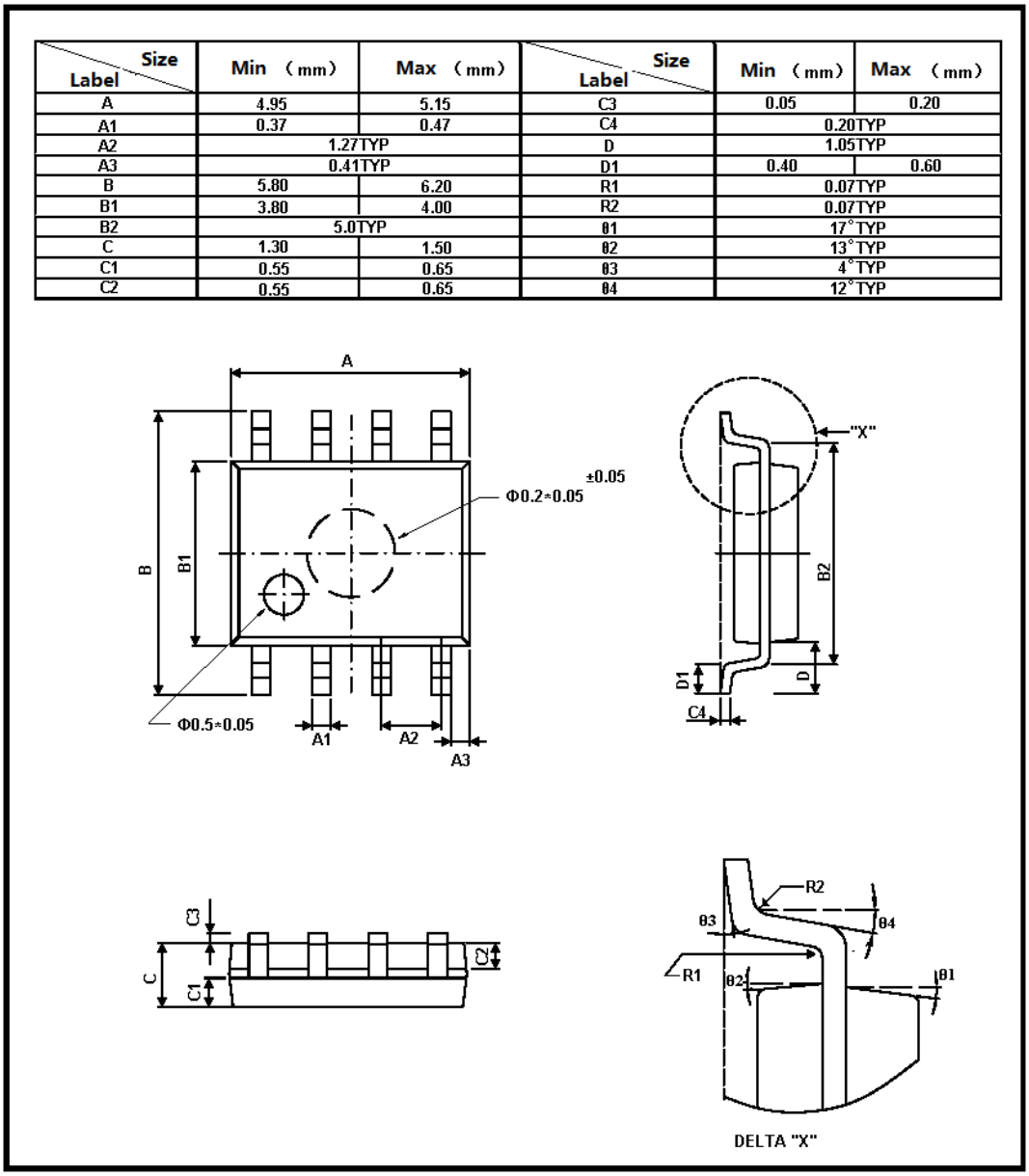
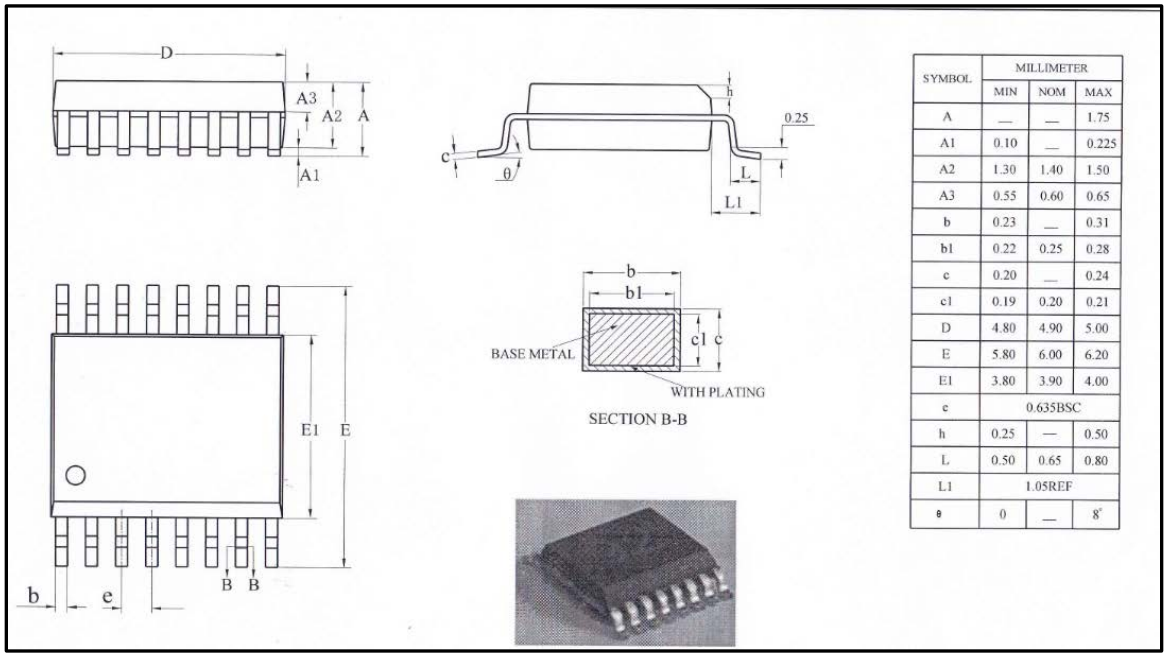


Figure 33 LW8110 Package

13.2 HLW8112 Package

HLW8112 is encapsulated with SSOP16. The encapsulation information is shown below.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.55	0.60	0.65
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	0.65	0.80
L1	1.05REF		
θ	0	—	8°

Figure 34 HLW8112 Package