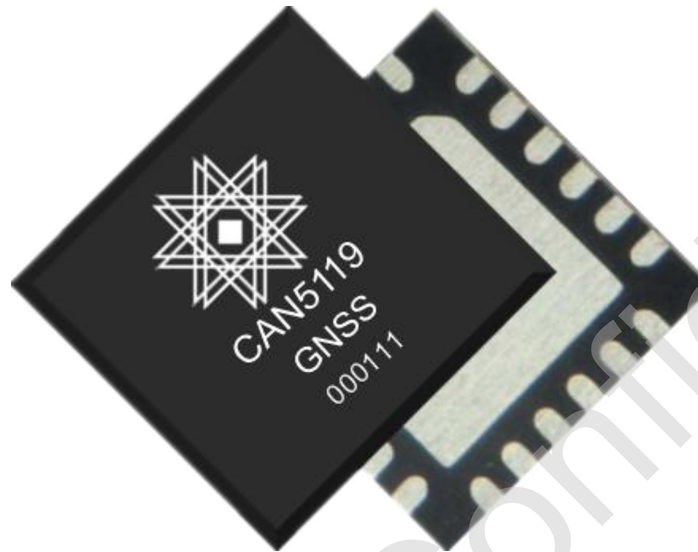

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CAN5119 Product Description

Rev 1.1 April 1, 2014

This datasheet is intended for customer's evaluation and application of the CAN5119 device. Under no circumstances it should be circulated outside the customer's company. This datasheet is preliminary and CanaanTek reserves the right to modify and to improve the data.

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PRODUCT DESCRIPTION

CAN5119 is a high-gain, low-noise amplifier (LNA) designed for GPS, Galileo, Glonass and Beidou GNSS applications. Designed in a standard low-cost RF CMOS process, the LNA achieves 16.0dB gain and 0.75dB noise figure. Together with the CanaanTek GNSS receiver CAN5115, CAN5119 forms the optimal RF front-end for the reception of GNSS satellites. Packaged in a 6-pin μDFN package, the CAN5119 sits on a small form factor PCB space. It can operate from a 1.6V to 3.6V single supply and draws only 5.5mA DC current. The shutdown leakage current is only 1uA.

APPLICATIONS

- Smartphone with GPS capability
- PNDs (Personal Navigation Devices)
- PMPs (Personal Media Players)
- Automobile Navigation Systems
- GNSS tracking systems
- GNSS industrial applications
- Software GPS
- iPad like Mobile PCs

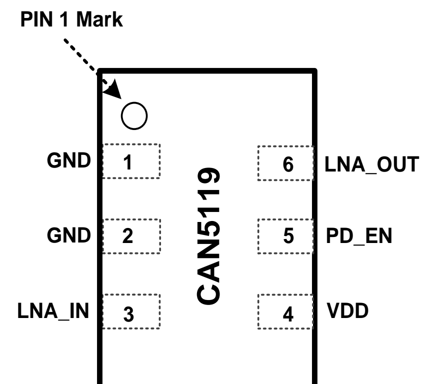
TECHNOLOGY

- Device in a small 1.45mmx1mm 6-pin uDFN RoHS-compliant package
- Integrated LDO
- Silicon CMOS 0.18um process with 1.8/3.3V operation

FEATURES

- Ultra-low-noise figure of 0.75dB
- High-power gain of 16.0dB
- Low-power of 5.5mA operated from a single 1.6V to 3.6V voltage
- Small footprint of 1.45mmx1mm
- Thin profile of 0.55mm
- Lead-free and RoHS-compliant package
- High integration with few off-chip BOM and low cost
- Temperature from –40° to 85° range

PIN ASSIGNMENT



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PIN CONNECTIONS AND INTERNAL BLOCK DIAGRAM

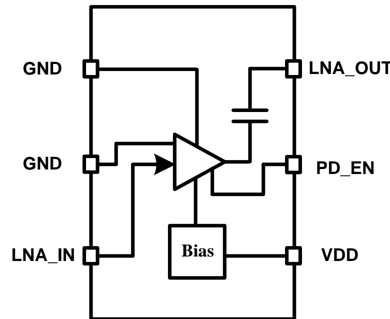

Figure 1 Block Diagram for LNA

Pin Out Description

Pin No.	Name	Description	Connection
1	GND	Ground connection	Connect to PCB ground plane.
2	GND	Ground connection	Connect to PCB ground plane.
3	LNA_IN	RF Input	Requires a DC-blocking capacitor and external matching components.
4	VDD	power supply for LNA	Supply Voltage.
5	PD_EN	Shut down Input	A logic-low disables the device.
6	LNA_OUT	RF Output	RF output. Connect either direct to saw filter input, or to match component using an inductor.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply Voltage	VDD	T_A=+25℃		4.0	V
Power Down Voltage	V_{PD_EN}	T_A=+25℃		4.0	V
LNA Max RF Input Power	P_{in}			0	dBm
ESD: HBM, 150pF/1.5KOhm	-		2.5		kV
Storage Temperature	T_{STG}		-40	+150	°C
Solder Reflow Temperature	T_{SLDR}			+260	°C

This device should be handled with care within the above stress ratings. This IC has ESD protection circuits within but must be handled and assembled according to the industry practice and at the ESD protected work platforms.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	T_A	-40	+25	+85	^{0}C
Supply Voltage	VDD	1.6	2.7	3.6	V
Power Down Turn-on Voltage	V_{PDon}	1.6	-	VDD	
Power Down Turn-off Voltage	V_{PDoff}	0	-	0.4	V

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, VDD = V_{PD_EN} = 2.7V, f_{in} = 1575.42MHz, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
circuit current	I_{cc}	No Signal	4.5	5.5	6.5	mA
Power Gain	G_p	Pin=-35dBm	14.5	16.0	17	dB
Noise Figure	NF		-	0.75	1.1	dB
Input Return Loss	RL_{in}		-	12	-	dB
Output Return Loss	RL_{out}		-	5.5	-	dB

STANDARD CHARACTERISTICS FOR REFERENCE

(T_A = +25℃, VDD = V_{PD_EN} = 2.7V, f_{in} = 1 575.42MHz, unless otherwise specified)

Parameter	Symbol	Test Conditions	Reference	Unit
Isolation	ISL		29	dB
Input 3rd Order Distortion Intercept Point	IIP_3	（Note1）	2	dBm
Gain 1 dB Compression Input Power	$P_{in(1dB)}$		-12.5	dBm

Note1: Measured with the two tones located at 5MHz and 10MHz offset from the center of the GPS band with -40dBm/tone.

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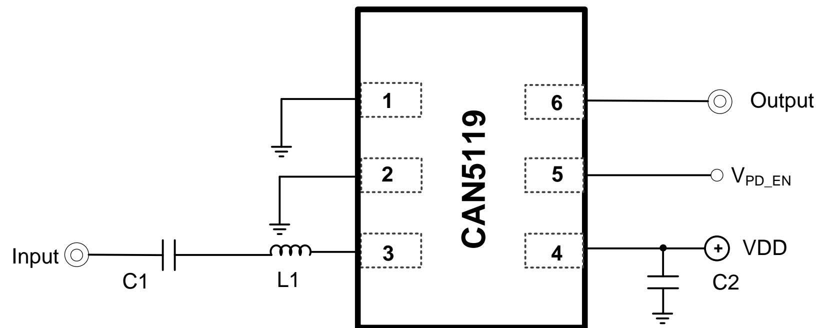
Typical Application Diagram



BOM LIST

BOM Descriptions	Symbol	Size	Value	Unit
Chip Capacitor	C1	0402	100	pF
Chip inductor	L1	0402	8.2	nH
Chip Capacitor	C2	0402	10	nF

Notes:

One inductor of 5.6nH is recommended to be in series with the output for better output return loss and higher gain.

These component values are for reference only and are subject to change with customer specific PCB layout design.

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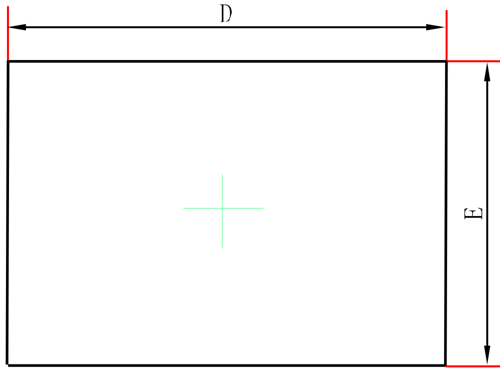
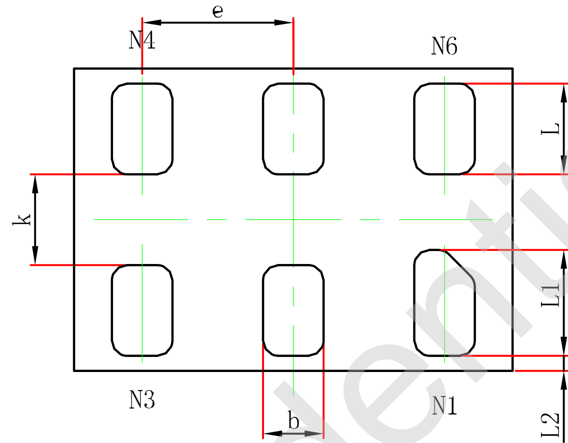
PACKAGE DIMENSIONS

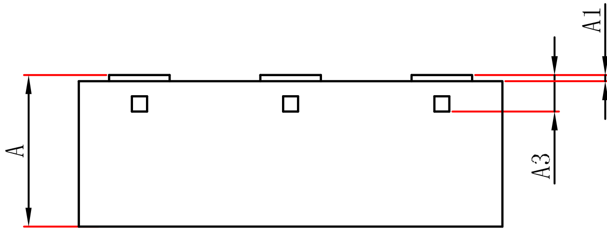
6-PIN PLASTIC TSON (UNIT: mm)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.110REF.		0.004REF.	
D	1.374	1.526	0.054	0.060
E	1		0.0394	
D1	——	——	——	——
E1	——	——	——	——
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.500TYP.		0.020TYP.	
L	0.250	0.350	0.010	0.014
L1	0.300	0.400	0.012	0.016
L2	0.000	0.100	0.000	0.004

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RECOMMANDED REFLOW PROFILE

Table2 Reflow Test Condition

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax)(ts)	 150℃ 200℃ 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3℃/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217℃ 60-150 seconds
Peak package body temperature (Tp) *	See classification temp in Table 3
Time (tp)** within 5℃ of the specified clsssification temperature (Tc)	30**seconds
Average ramp-down rate (Tp to Tsmax)	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum. **Tolerance for time at peak profile temperature (tp) is defined as a supplier minimum and a user maximum.	

Remark: All temperatures refer to the package body surface temperature. The highest temperature of reflow profile can not exceed 265℃.

Note 1: All temperatures refer to the center of the package，measured on the package body surface that is facing up during assembly reflow (e.g.，live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e.，dead-bug)，Tp shall be within ±2℃ of the live-bug Tp and still meet the Tc requirements，otherwise，the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table2. For example，if Tc is 260℃ and time tp is 30 seconds，this means the following for the supplier and the user. For a supplier: The peak temperature must be at least 260℃ .The time above 255℃ must be at least 30 seconds. For a user: The peak temperature must not exceed 260℃. The time above 255℃ must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Note4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020，JESD22-A112 (rescinded)，IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

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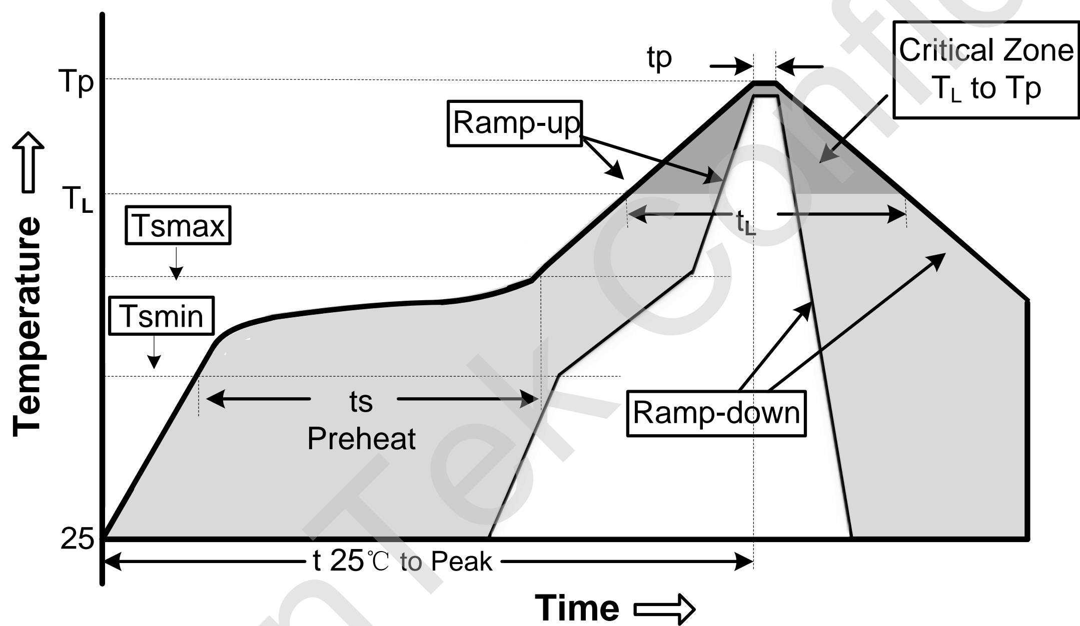
Table 3 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3 < 350	Volume mm3 350 - 2000	Volume mm3 > 2000
< 1.6 mm	260℃	260℃	260℃
1.6 mm - 2.5 mm	260℃	250℃	245℃
> 2.5 mm	250℃	245℃	245℃

Reflow Profile



The reflow profile shown above should not be exceeded, since excessive temperatures or transport times during reflow can damage the chip.

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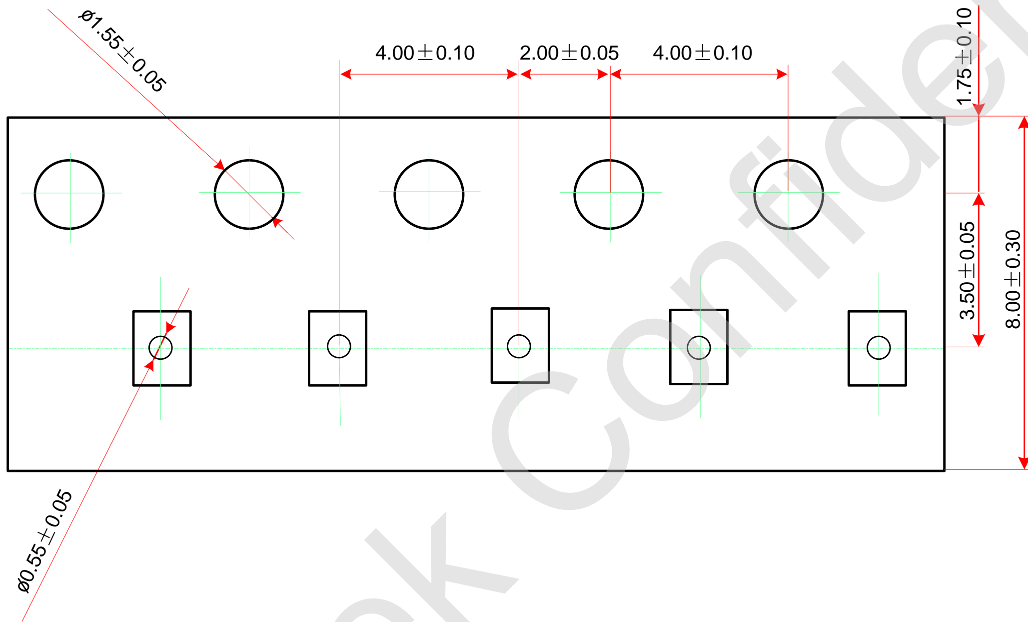
PACKING SPEC

PKG	TAPE	REEL	BOX	PCS/REEL	REEL/BOX	PCS/BOX	BOX/CARTON	PCS/CARTON
MIS1.45X1	IC-ZD-26	7''(IC-JP-05)	SOT23	3000	10	30000	4	120000

Tape & Real Dimension



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