3-Pin Supply Voltage Supervisors

Check for Samples: TLV809J25, TLV809L30, TLV809K33, TLV809I50

FEATURES

- **3-Pin SOT23 Package**
- **Supply Current: 9 µA (Typical)**
- **Precision Supply Voltage Monitor: 2.5 V, 3 V, 3.3 V, 5 V**
- **Power-On Reset Generator with Fixed Delay Time of 200 ms**
- **Pin-for-Pin Compatible with MAX809**
- **Temperature Range: –40°C to +85°C**

APPLICATIONS

- **DSPs, Microcontrollers, and Microprocessors**
- **Wireless Communication Systems**
- **Portable/Battery-Powered Equipment**
- **Programmable Controls**
- **Intelligent Instruments**
- **Industrial Equipment**
- **Notebook and Desktop Computers**
- **Automotive Systems**

DESCRIPTION

The TLV809 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD}) becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time ($t_{d(typ)}$ = 200 ms) starts after V_{DD} has risen above the threshold voltage, V_{IT}. When the supply voltage drops below the V_{IT} threshold voltage, the output becomes active (low) again. No external components are required. All the devices in this family have a fixed sense-threshold voltage (V_{IT}) set by an internal voltage divider.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23 package. The TLV809 devices are characterized for operation over a temperature range of –40°C to +85°C.

TLV809
DBV/DBZ Packages

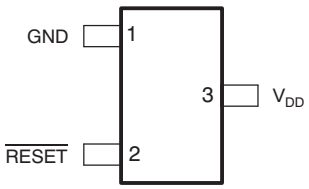
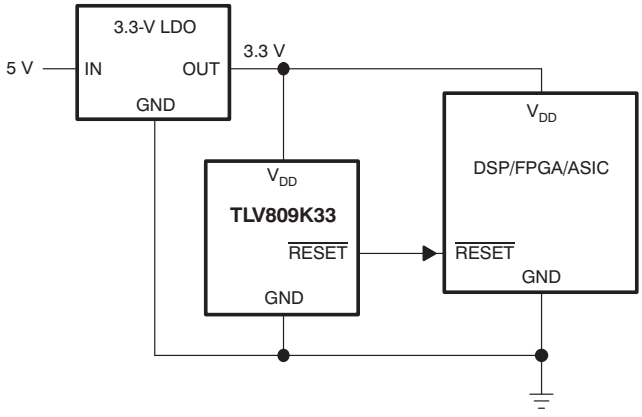


Figure 1. TYPICAL APPLICATION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	THRESHOLD VOLTAGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED OPERATING TEMPERATURE	PACKAGE MARKING	ORDERING INFORMATION	TRANSPORT MEDIA, QUANTITY
TLV809J25	2.25 V	SOT23-3	DBV	–40°C to +85°C	VTCI	TLV809J25DBVR	Tape and Reel, 3000
						TLV809J25DBVT	Tape and Reel, 250
			DBZ	–40°C to +85°C	BCMT	TLV809J25DBZR	Tape and Reel, 3000
						TLV809J25DBZT	Tape and Reel, 250
TLV809L30	2.64 V	SOT23-3	DBV	–40°C to +85°C	VTXI	TLV809L30DBVR	Tape and Reel, 3000
						TLV809L30DBVT	Tape and Reel, 250
			DBZ	–40°C to +85°C	BCMZ	TLV809L30DBZR	Tape and Reel, 3000
						TLV809L30DBZT	Tape and Reel, 250
TLV809K33	2.93 V	SOT23-3	DBV	–40°C to +85°C	VTRI	TLV809K33DBVR	Tape and Reel, 3000
						TLV809K33DBVT	Tape and Reel, 250
			DBZ	–40°C to +85°C	BCMX	TLV809K33DBZR	Tape and Reel, 3000
						TLV809K33DBZT	Tape and Reel, 250
TLV809I50	4.55 V	SOT23-3	DBV	–40°C to +85°C	VTBI	TLV809I50DBVR	Tape and Reel, 3000
						TLV809I50DBVT	Tape and Reel, 250
			DBZ	–40°C to +85°C	BCMV	TLV809I50DBZR	Tape and Reel, 3000
						TLV809I50DBZT	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted) .

		VALUE	UNIT
V_{DD}	Supply voltage(2)	7	V
	All other pins(2)	–0.3 to 7	V
I_{OL}	Maximum low output current	5	mA
I_{OH}	Maximum high output current	–5	mA
I_{IK}	Input clamp current ($V_I < 0$ or $V_I > V_{DD}$)	±20	mA
I_{OK}	Output clamp current ($V_O < 0$ or $V_O > V_{DD}$)	±20	mA
T_A	Operating free-air temperature range	–40 to +85	°C
T_{stg}	Storage temperature range	–65 to +150	°C
	Soldering temperature	+260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t = 1000h continuously

THERMAL INFORMATION

THERMAL METRIC(1)		TLV809 DBV 3 PINS	TLV809 DBZ 3 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	242.1	286.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	213.0	105.6	
θ_{JB}	Junction-to-board thermal resistance	123.4	124.4	
ψ_{JT}	Junction-to-top characterization parameter	45.7	25.8	
ψ_{JB}	Junction-to-board characterization parameter	130.9	107.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	—	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

At specified temperature range (unless otherwise noted).

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2	6	V
T_A	Operating free-air temperature range	–40	+85	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 2.5 V to 6 V,	I_{OH} = –500 µA	V_{DD} – 0.2			V
			V_{DD} = 3.3 V,	I_{OH} = –2 mA	V_{DD} – 0.4			
			V_{DD} = 6 V,	I_{OH} = –4 mA	V_{DD} – 0.4			
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V,	I_{OH} = 500 µA			0.2	V
			V_{DD} = 3.3 V,	I_{OH} = 2 mA			0.4	
			V_{DD} = 6 V,	I_{OH} = 4 mA			0.4	
	Power-up reset voltage(1)		V_{DD} ≥ 1.1 V,	I_{OL} = 50 µA			0.2	V
V_{IT-}	Negative-going input threshold voltage(2)	TLV809J25	T_A = –40°C to 85°C		2.20	2.25	2.30	v
		TLV809L30			2.58	2.64	2.70	
		TLV809K33			2.87	2.93	2.99	
		TLV809I50			4.45	4.55	4.65	
V_{hys}	Hysteresis	TLV809J25				30		mV
		TLV809L30				35		
		TLV809K33				40		
		TLV809I50				60		
I_{DD}	Supply current		V_{DD} = 2 V,	Output unconnected		9	12	µA
			V_{DD} = 6 V,	Output unconnected		20	25	
C_i	Input capacitance		V_I = 0 V to V_{DD}			5		pF

(1) The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_{r,\ VDD}$ ≥ 15 ms/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (0.1-µF ceramic) should be placed near the supply terminals.

TIMING REQUIREMENTS

At R_L = 1 MΩ, C_L = 50 pF, T_A = +25°C.

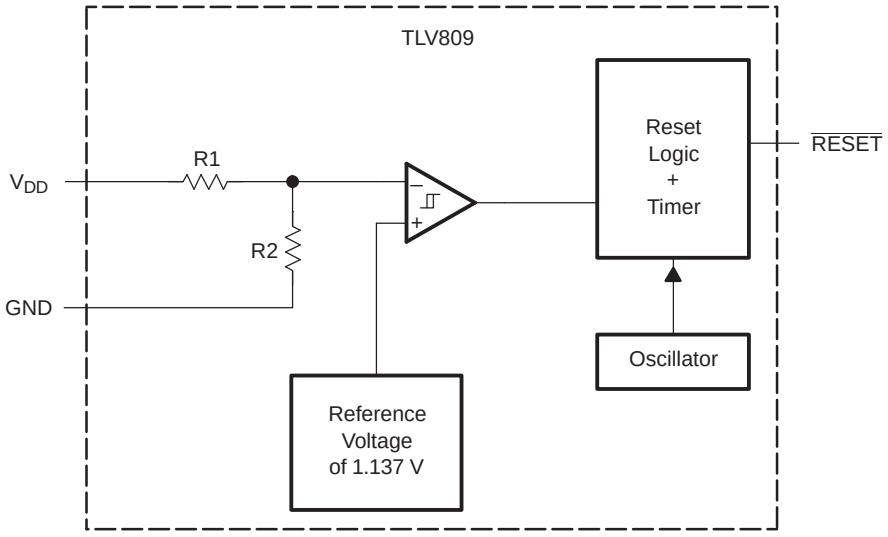
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width at V_{DD}	$V_{DD} = V_{IT-} + 0.2$ V, $V_{DD} = V_{IT-} - 0.2$ V	3			µs

SWITCHING CHARACTERISTICS

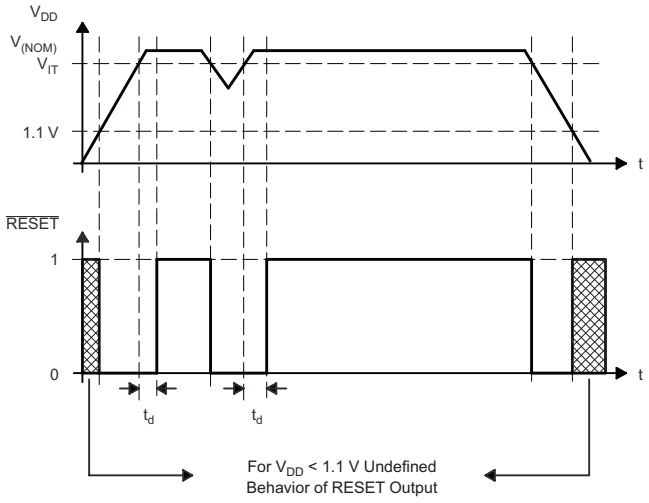
At R_L = 1 MΩ, C_L = 50 pF, T_A = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geq V_{IT-} + 0.2$ V; see timing diagram	120	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{\text{RESET}}$ delay	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V		1		µs

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM



TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

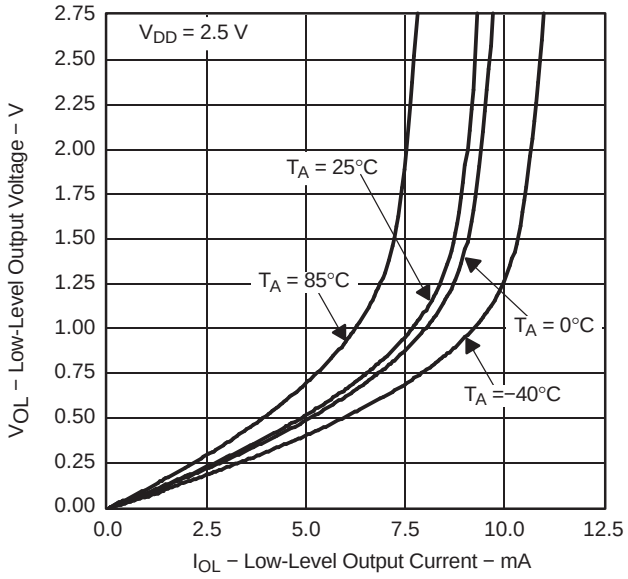


Figure 2.

SUPPLY CURRENT vs SUPPLY VOLTAGE

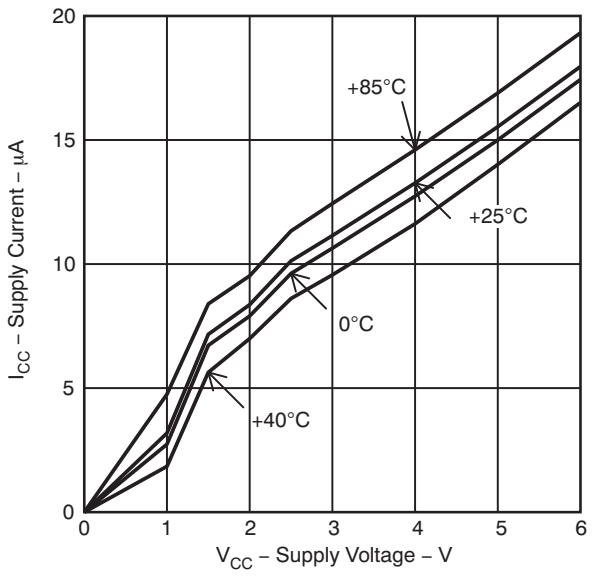


Figure 3.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

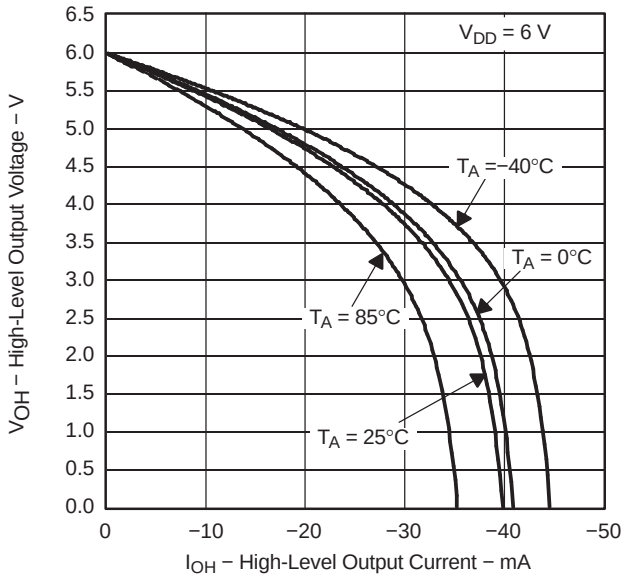


Figure 4.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

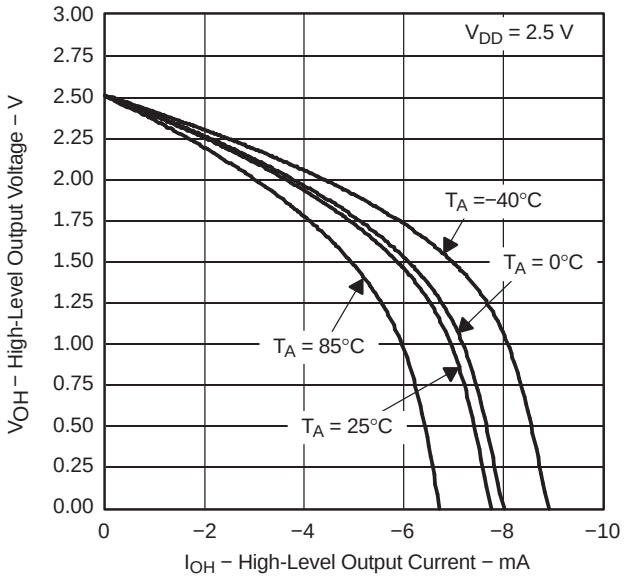


Figure 5.

TYPICAL CHARACTERISTICS (continued)

NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT V_{DD}

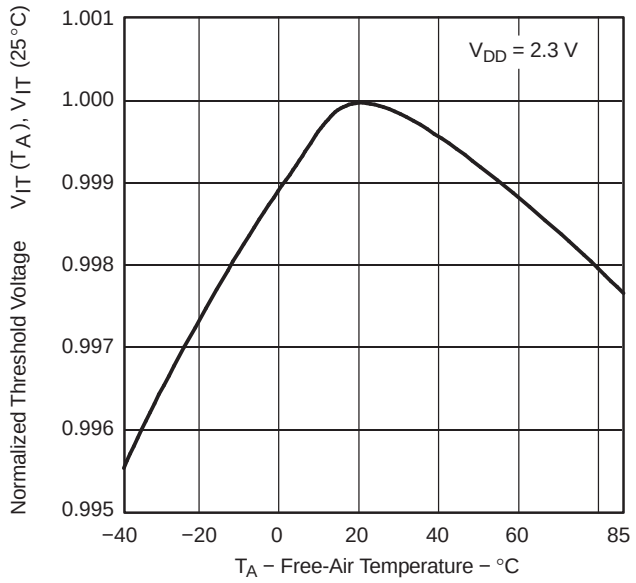


Figure 6.

MINIMUM PULSE DURATION AT V_{DD} vs V_{DD} THRESHOLD OVERDRIVE VOLTAGE

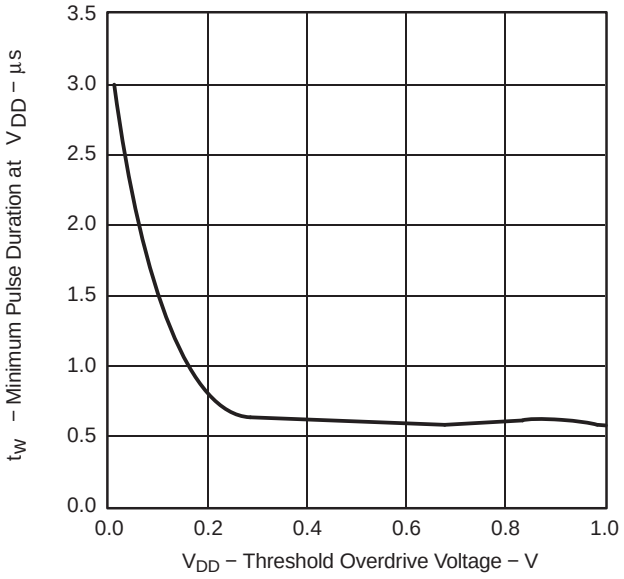


Figure 7.

REVISION HISTORY

NOTE: Page numbers from previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2010) to Revision C **Page**

- Changed TLV809L30 DBZ ordering information column in Package/Ordering Information table 2
- Changed TLV809K33 DBZ ordering information column in Package/Ordering Information table 2
- Changed first TLV809I50 DBZ ordering information entry in Package/Ordering Information table 2

Changes from Revision A (July 2010) to Revision B **Page**

- Updated document format to current standards 1
- Added DBZ package to pinout figure 1
- Added DBZ package to *Package/Ordering Information* table 2
- Added *Thermal Information* table 2
- Changed Figure 3 5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV809I50DBVR	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTBI	Samples
TLV809I50DBVT	ACTIVE	SOT-23	DBV	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTBI	Samples
TLV809I50DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCMV	Samples
TLV809I50DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCMV	Samples
TLV809J25DBVR	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTCI	Samples
TLV809J25DBVT	ACTIVE	SOT-23	DBV	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTCI	Samples
TLV809J25DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCMT	Samples
TLV809J25DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCMT	Samples
TLV809K33DBVR	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTRI	Samples
TLV809K33DBVT	ACTIVE	SOT-23	DBV	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTRI	Samples
TLV809K33DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCMX	Samples
TLV809K33DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCMX	Samples
TLV809L30DBVR	ACTIVE	SOT-23	DBV	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTXI	Samples
TLV809L30DBVT	ACTIVE	SOT-23	DBV	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VTXI	Samples
TLV809L30DBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCMZ	Samples
TLV809L30DBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCMZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

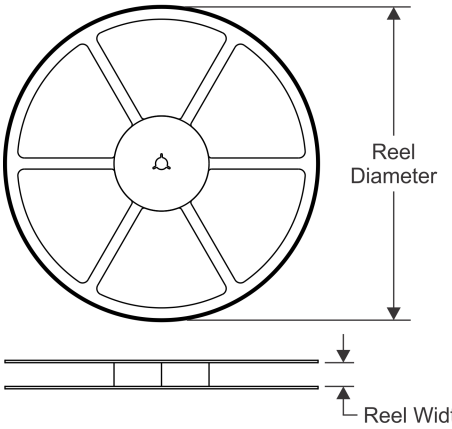
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

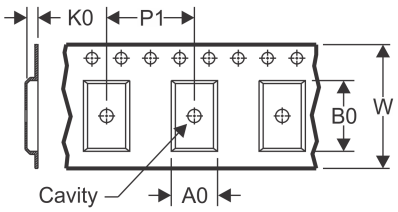
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

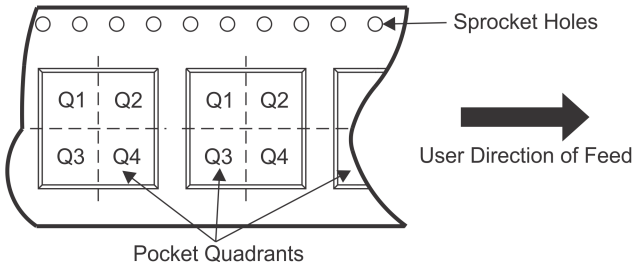


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

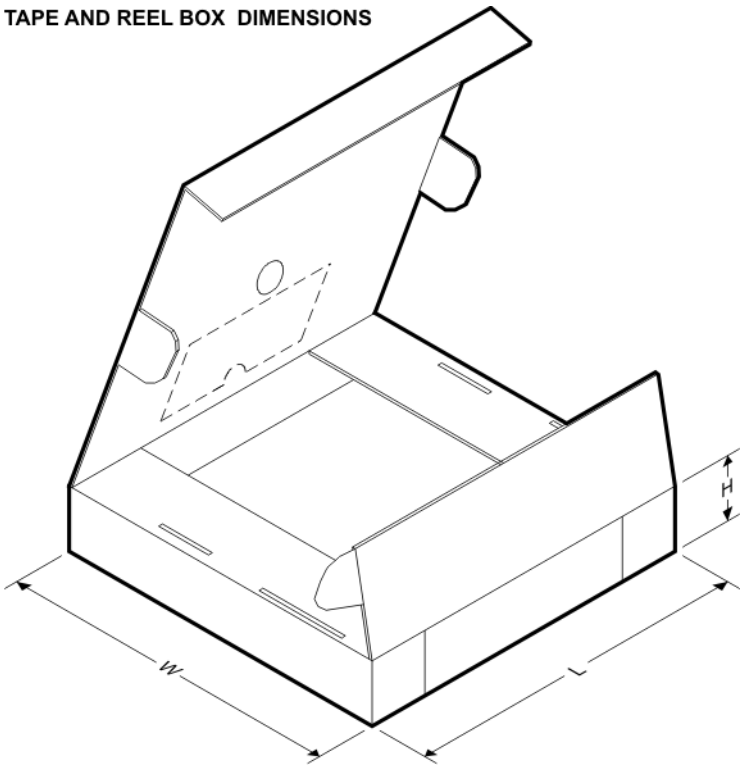
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV809I50DBVR	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809I50DBVT	SOT-23	DBV	3	250	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809I50DBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809I50DBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809J25DBVR	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809J25DBVT	SOT-23	DBV	3	250	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809J25DBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809J25DBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809K33DBVR	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809K33DBVT	SOT-23	DBV	3	250	178.0	8.4	3.3	3.2	1.47	4.0	8.0	Q3
TLV809K33DBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809K33DBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809L30DBVR	SOT-23	DBV	3	3000	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809L30DBVT	SOT-23	DBV	3	250	180.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TLV809L30DBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV809L30DBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

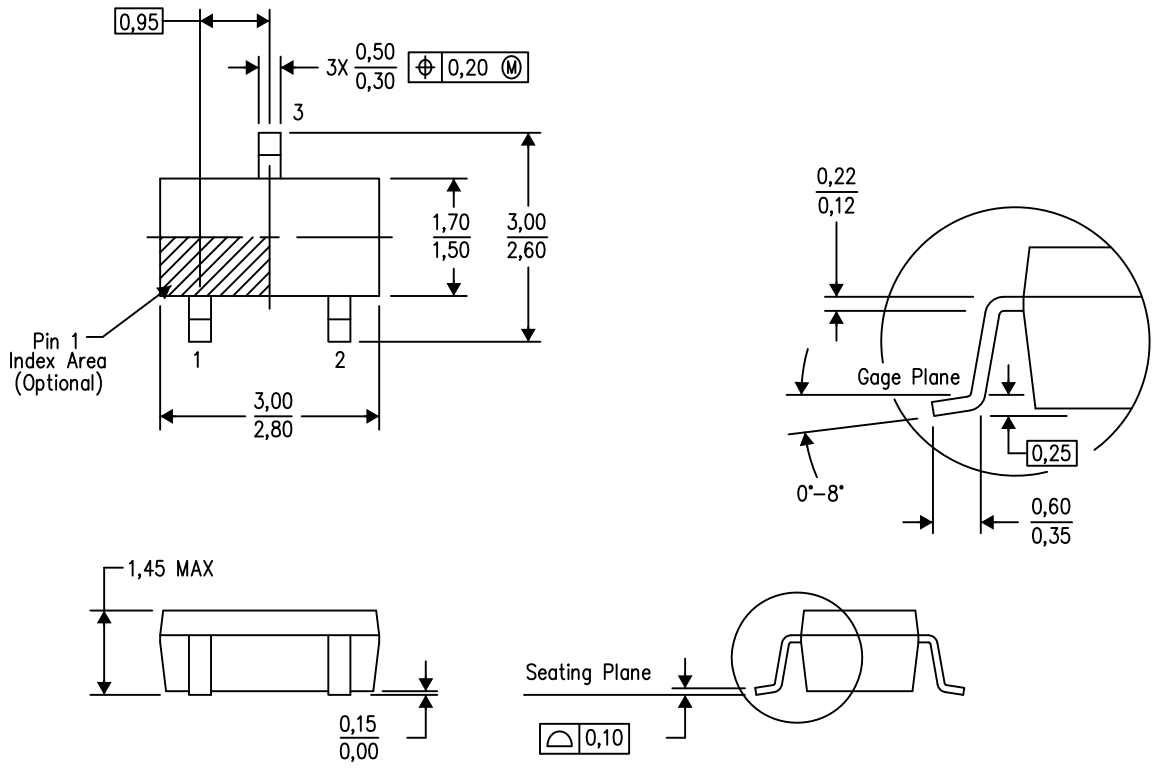
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV809I50DBVR	SOT-23	DBV	3	3000	182.0	182.0	20.0
TLV809I50DBVT	SOT-23	DBV	3	250	182.0	182.0	20.0
TLV809I50DBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV809I50DBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV809J25DBVR	SOT-23	DBV	3	3000	182.0	182.0	20.0
TLV809J25DBVT	SOT-23	DBV	3	250	182.0	182.0	20.0
TLV809J25DBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV809J25DBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV809K33DBVR	SOT-23	DBV	3	3000	180.0	180.0	18.0
TLV809K33DBVT	SOT-23	DBV	3	250	180.0	180.0	18.0
TLV809K33DBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV809K33DBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV809L30DBVR	SOT-23	DBV	3	3000	182.0	182.0	20.0
TLV809L30DBVT	SOT-23	DBV	3	250	182.0	182.0	20.0
TLV809L30DBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV809L30DBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0

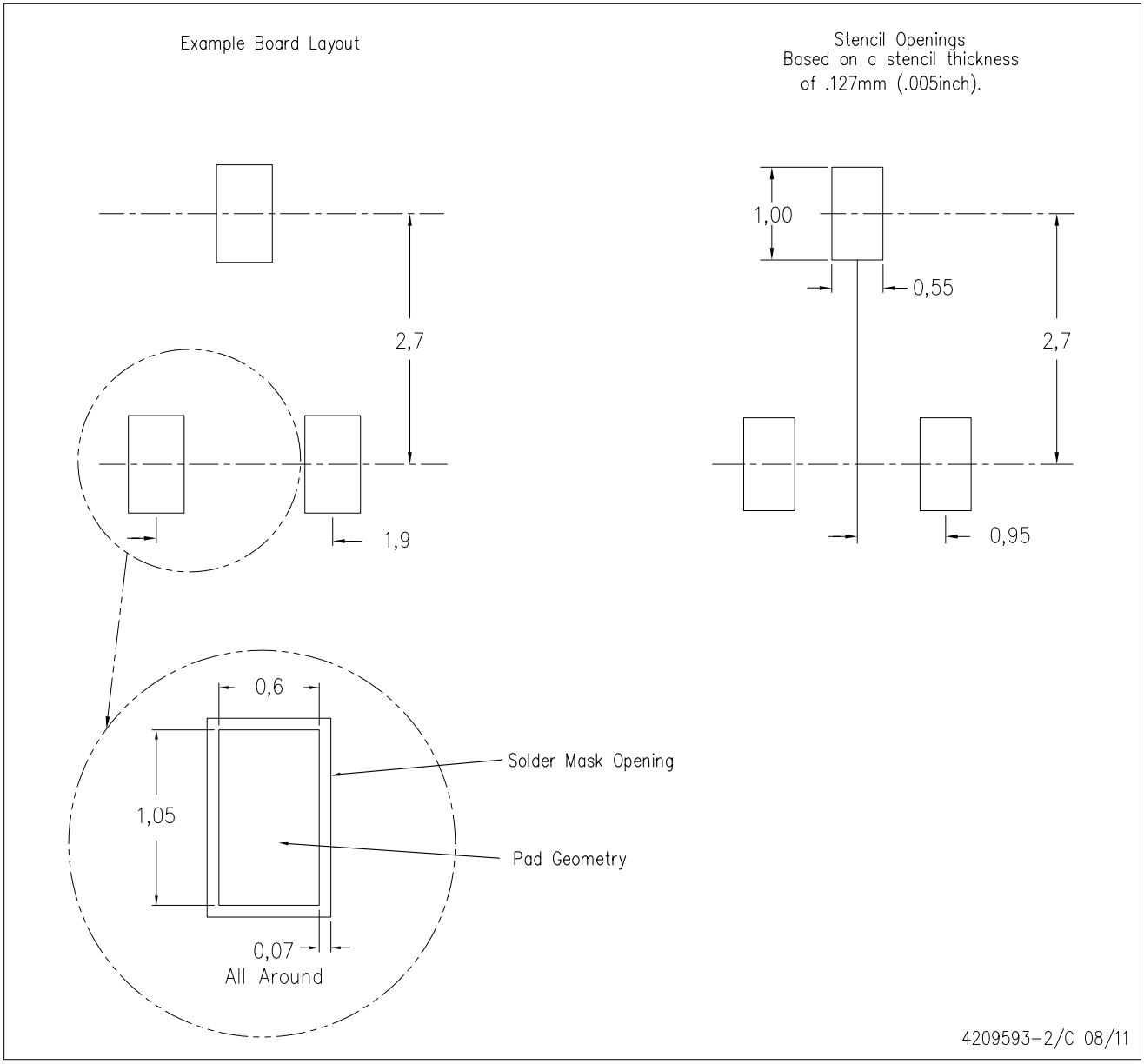
DBV (R–PDSO–G3) PLASTIC SMALL–OUTLINE PACKAGE



4073253–2/N 12/14

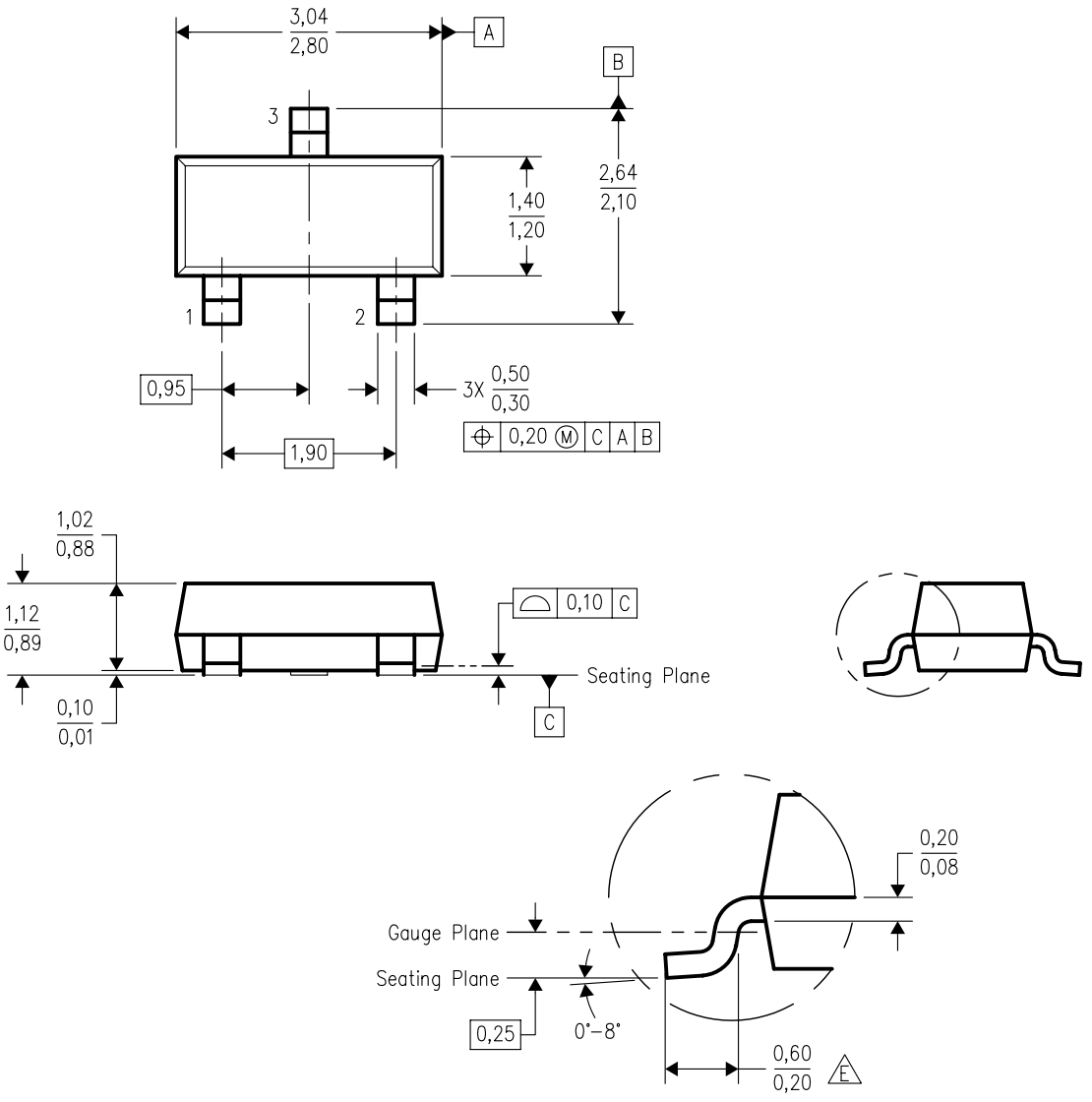
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

DBV (R–PDSO–G3) PLASTIC SMALL OUTLINE



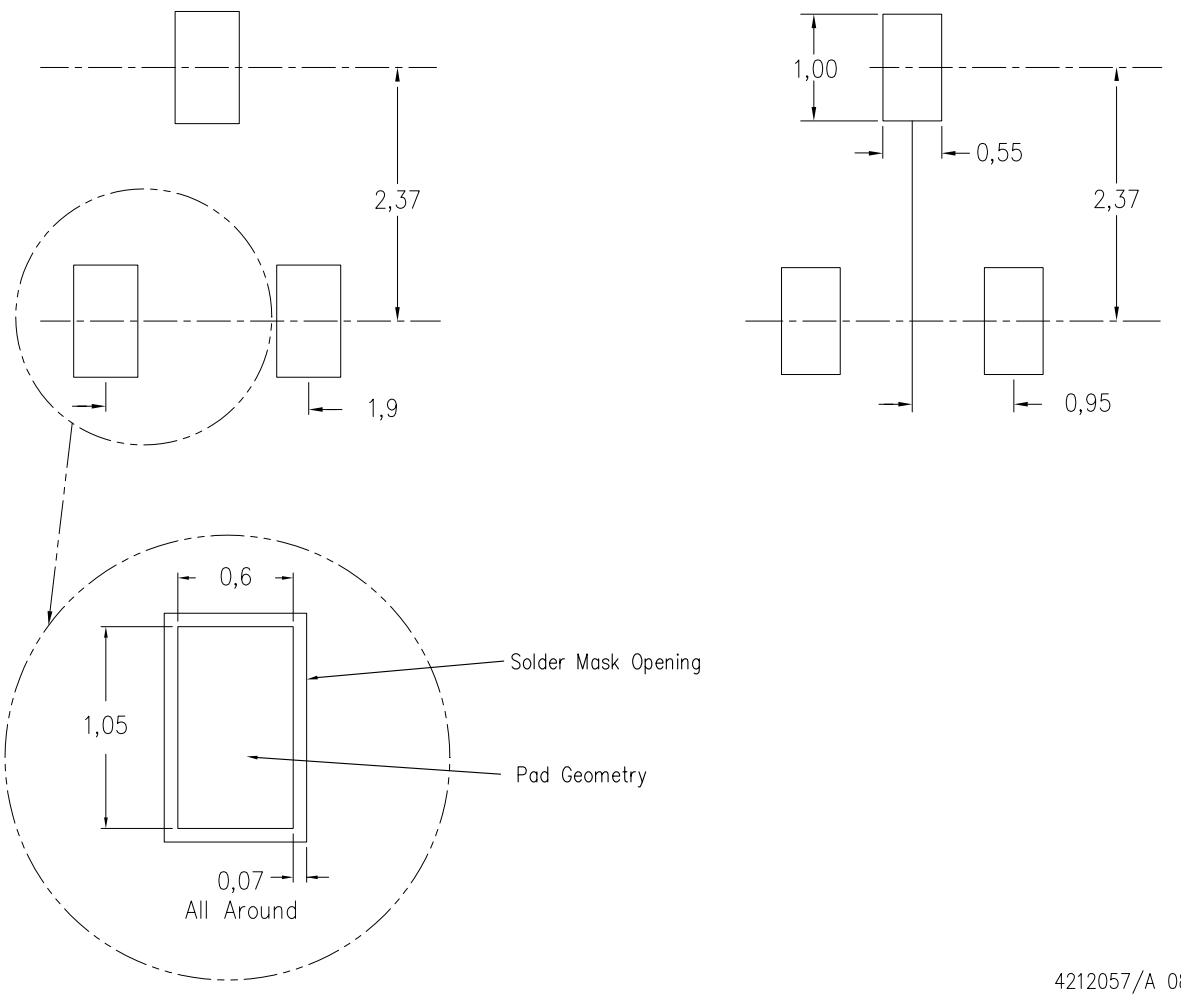
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBZ (R–PDSO–G3) PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Lead dimensions are inclusive of plating.
D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
E. Falls within JEDEC TO–236 variation AB, except minimum foot length.

DBZ (R–PDSO–G3) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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